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Design Analysis of one-sided Schmitt-trigger-based 9T SRAM cell for near-threshold operation

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ABSTRACT:

This study introduces a novel 9T static random access memory (SRAM) cell utilizing a one-sided Schmitt-trigger design to enhance energy efficiency, while ensuring robust read stability, write ability, and hold stability. Unlike conventional approaches, this design doesn't rely on a write-back scheme. The key innovation lies in employing a one-sided Schmitt-trigger inverter along with a single bit-line structure, significantly enhancing read stability yield. Moreover, enhancements to write ability yield are achieved through selective power gating and a Schmitt-trigger inverter write assist technique, effectively managing the trip voltage of the Schmitt-trigger inverter. Compared to existing designs like Chang's 10T SRAM, Schmitt-trigger-based 10T SRAM, and MH's 9T SRAM cells on 22-nm FinFET technology, the proposed Schmitt-trigger-based 9T SRAM cell demonstrates notable improvements in area and energy consumption. Specifically, it occupies 0.79 times the area and consumes 0.31 times the energy of Chang's 10T SRAM, 0.77 times the area and 0.68 times the energy of the Schmitt-trigger-based 10T SRAM, and 0.79 times the area and 0.90 times the energy of MH's 9T SRAM.

Key terms: bit interleaving, low energy, near-threshold, Schmitt-trigger, static random access memory (SRAM)

INTRODUCTION

OW energy consumption has become important in the design of system-on-chips (SoCs), such as bio implants, mobile devices, self-powered wireless sensors, and energy harvesting devices, because they operate with limited energy from a battery or harvesting. Because static random access memory (SRAM) occupies a significant area on the SoC [1], reducing the energy consumption of SRAM is a critical way to reduce the energy consumption of the SoC. The most effective way to reduce energy consumption is to reduce power by scaling down the supply voltage (V_{DD}). As the V_{DD} scales down, the power decreases quadratically [2]. However, as V_{DD} scales down,

In the sub-threshold voltage (V_{th}) region where V_{DD} is lower than V_{th}, the delay increases

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exponentially. Thus, the energy consumption is increased because of the signifi- cantly increased static energy consumption, even though very low power is achieved. Operation in the near-V_{th} region where V_{DD} is slightly higher than V_{th} can achieve a large power

EXISTING SYSTEM:

On Floods so far, several literature studies have been conducted in order to gain the understanding and the knowledge to implement an advance flood monitoring system. L. Siew Khaun et al were able to invent a system that could detect the water depth when it is over the standard level as specified by the sensor. This paper was then placed where a flood always occurs. This paper had the ability to use the flashlight as a warning and also inform the control room. In this paper Radiofrequency transmitter and receiver wereused for information communication.

the water level monitoring was done using the android smart and ultrasonicsensors. In this paper, the information about the flooding would be availableon android applications. This system had an error rate of 1.121%.

PROPOSED SYSTEM:

Various SRAM cells (MH's 9T [5], Chang's 10T [7], conventional 8T [8], write- and read-enhanced (WRE) 9T [9], ST 10T [10], ST 11T [11]) have been proposed for near-V_{th} operation as shown in Fig. 1. The conventional 6T and 8T, WRE 9T, Chang's 10T, and MH's 9T SRAM cells have cross-coupled standard inverters, while ST 10T and ST 11T SRAM cells have cross-coupled ST inverters. In addition, the SRAM cells will be classified into read-disturbance and read-disturbance-free cells, depending on whether the storage node suffers from read disturbance.

The conventional 6T SRAM cell can be classified into read- disturbance cell because the read disturbance from BL or BLB can flip the stored data. The conventional 8T SRAM cell adds a read buffer to resolve a read disturbance problem. Because the read buffer decouples the storage node from read BL, the conventional 8T SRAM cell has the same read stability as hold stability. Thus, the conventional 8T SRAM cell ensures sufficient read stability. The WRE 9T SRAM cell improves leakage current of the read buffer as well as write ability by using power gating. During the write operation, however, the conventional 8T and WRE 9T SRAM cells experience read disturbance from BL or BLB. Thus, the bit-interleaving structure can be applied only by using write-back scheme that increases the delay, energy consumption, and area.

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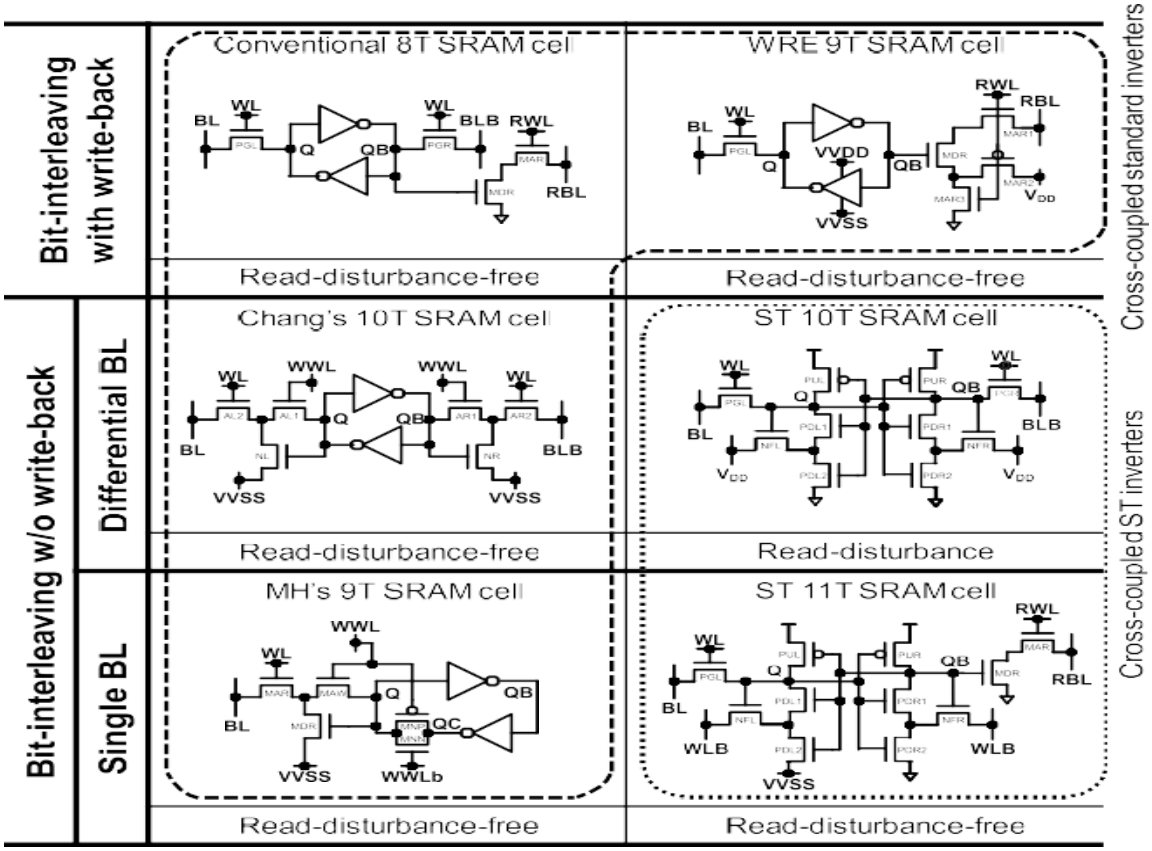

Schematics of the previous SRAM cells.

PROPOSED ST 9T SRAM CELL

the schematic and operational timing diagram of the proposed ST 9T SRAM cell having a single BL structure. The proposed ST 9T SRAM cell consists of a cross-coupled structure of a standard inverter with stacked transistors (PUL1, PUL2, PDL1, PDL2), an ST inverter

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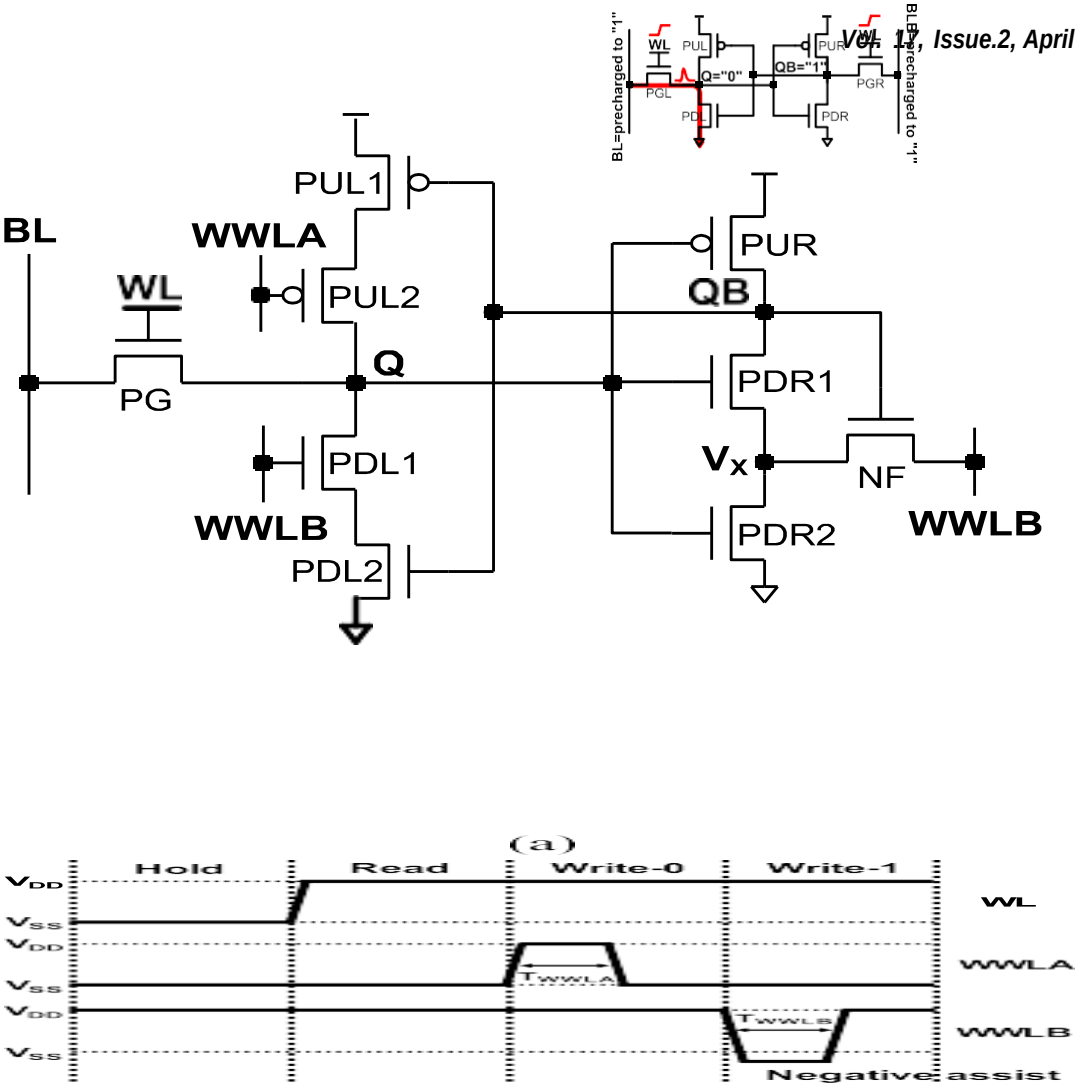

Fig. 2. (a) Schematic, (b) operation timing diagram of the proposed ST 9T SRAM cell.

voltage than the standard inverter. This is because the strength of PD1 is weakened by the V_X increased through the feedback transistor NF. Thus, when the storage node is bumped by a read disturbance, the ST inverter is more robust to the read disturbance than the standard inverter

shows the bumped storage node in the read-disturbance cells. The ST 10T and proposed ST 9T SRAM cells improve the read stability through the benefit of ST inverter. Furthermore, the proposed ST 9T SRAM cell has a larger read stability than ST 10T SRAM cell where the ST inverters are cross-coupled. The reason is as follows. When the node Q storing the data "0" in the ST 10T SRAM cell is bumped by the read disturbance, NFL is slightly turned ON and the strength of PDL1 is weakened by the increase in V_{XL} through NFL.

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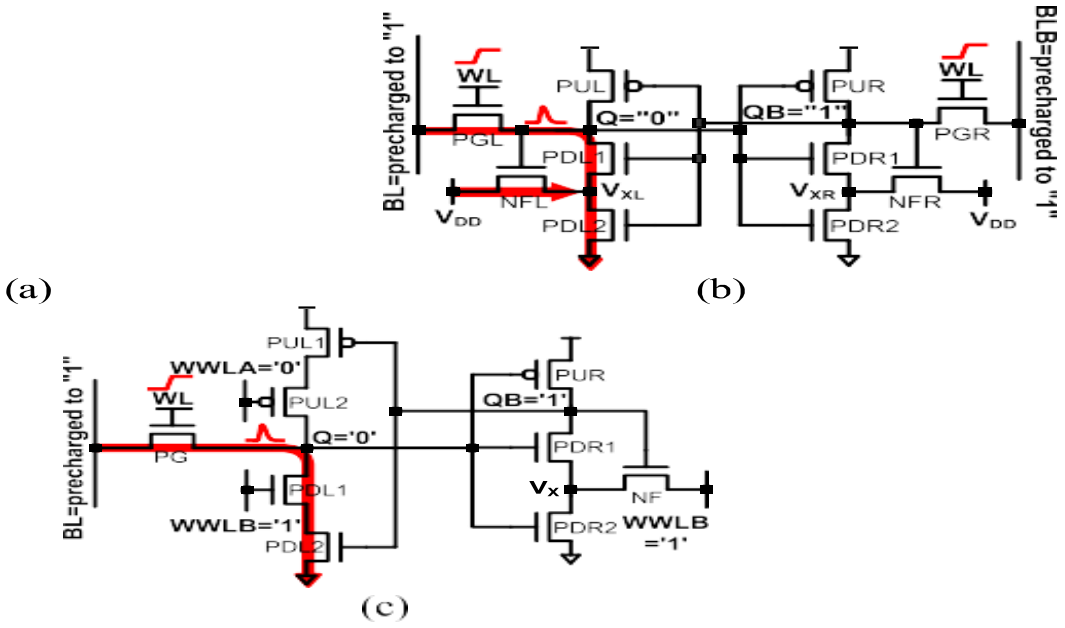

Read operation (a) in conventional 6T, (b) ST 10T, and (c) theproposed ST 9T SRAM cells.

operation, the column-based WWLB remains "1", the write driver drives BL to "0", and the WL is enabled. As the column-based WWLA is changed to "1" to disconnect the path from the V_{DD} power source by turning off PUL2, nodeQ storing data "1" is power-gated. The power-gated Q node is driven to "0" through the turned-on PG, and the ST inverteris flipped. The column-based WWLA is reset to "0" after the stored data of node QB is flipped. The pulse width of WWLA (T_{WWLA}) is determined considering the column half-selected cell, which will be discussed in detail in the following section. The proposed ST 9T SRAM cell adopts a single PG insteadof the series PGs used in Chang's 10T or MH's 9T SRAM cells, and disconnects the path from the V_{DD} power source by turning off PUL2 in the write-0 operation. As a result, the proposed ST 9T SRAM cell achieves sufficient write-0 ability.

Parameter	NMOS	PMOS
Gate length	34 nm	34 nm
Equivalent oxide thickness	0.9 nm	0.9 nm
Fin thickness	8 nm	8 nm
Fin height	34 nm	34 nm
On-current	880 μA/μm	780 μA/μm
Off-current	1 nA/μm	1 nA/μm
Sub-threshold swing	69 mV/dec	72 mV/dec
DIBL	46 mV/V	50 mV/V
Threshold voltage (V_{th})[a]	230 mV (Sat.) 264 mV (Lin.)	245 mV (Sat.) 283 mV (Lin.)
C_{gg}	1.47 fF/μm	
C_d	0.33 fF/μm	

[a] Vth in the saturation and linear model are measured as V_{GS} when the drain current per effective width is 10^{-5} A/μm with $|V_{DS}| = V_{DD}$ and $|V_{DS}| = 0.05V$.

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RESULTS AND DISCUSSIONS:

summarizes the comparison of the previous and proposed ST 9T SRAMs at each V_{min_energy}. A figure of merit (FOM) is often introduced to compare digital circuits that perform the same function using different designs. To consider both energy and performance, an energy-delay product (EDP) is usually used. An EDP with the same weight for delay and energy do not reflect the importance of delay and energy according to the V_{DD}. Thus, the weights of delay and energy should be considered according to the V_{DD}. In the near-V_{th} region, the EDP is calculated by following equation according

TABLE IV

COMPARISON IN 22-nm FINFET TECHNOLOGY

SRAM cell	Chang's	ST 10T	MH's	Proposed
V_{min_energy}	0.40 V	0.46 V	0.46 V	0.48 V
Cell area	0.191 μm²	0.197 μm²	0.191 μm²	0.151 μm²
Read stability yield	8.1σ	5.0σ	9.0σ	5.4σ
Read delay	34.7 ns	4.6 ns	24.0 ns	8.2 ns
Write ability yield	5.0σ	5.0σ	5.0σ	5.0σ
Write assist voltage (row)	0.11 V	0.00 V	0.09 V	0.02 V
Write assist voltage (column)[a]	0.11 V	0.14 V	0.09 V	0.10 V
Read energy	1.50 pJ	0.63 pJ	0.45 pJ	0.38 pJ
Write energy	0.79 pJ	0.78 pJ	0.71 pJ	0.87 pJ
Total energy	1.41 pJ	0.65 pJ	0.49 pJ	0.44 pJ
Normalized near-V_{th} EDP	4.30	1.31	1.37	1.00

[a] Applied write assist voltage per column.

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CONCLUSIONS:

Low energy consumption has become important for bio implants and mobile devices because they need to operate with limited energy. For minimization of the energy consumption, it is important to operate the SRAM in near-V_{th} region. This paper proposed a one-sided ST 9T SRAM cell with low energy consumption, and high read stability, write ability, and hold stability yields in the near-V_{th} region. The read stability yield was improved in the proposed ST 9T SRAM cell by using a cross-coupled structure of standard and ST inverters. In addition, the proposed ST 9T SRAM cell ensured a 5σ target write ability yield by using selective power gating and a novel negative V_{WWLB} assist technique that controlled the trip voltage of the ST inverter. The proposed ST 9T SRAM cell has a smaller area than Chang's 10T, the ST 10T, and MH's 9T SRAM cells. The proposed ST 9T SRAM consumes much less energy than Chang's 10T, the ST 10T, and MH's 9T SRAMs at each V_{min_energy}, although it has a larger read delay owing to the single BL structure. As a result, the proposed ST 9T SRAM cell has the best near-V_{th} EDP

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