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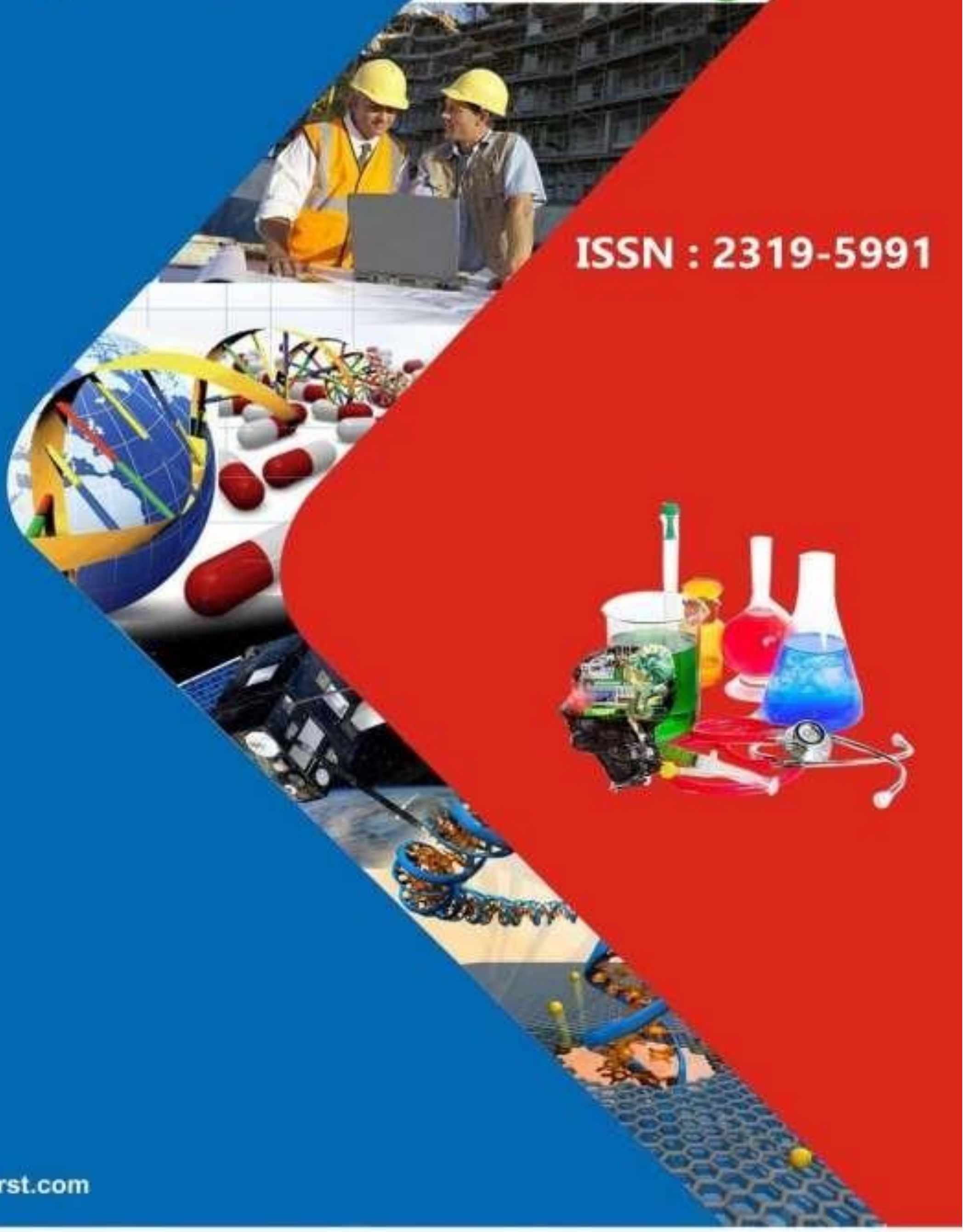

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REALIZATION OF HIGH-PERFORMANCE APPROXIMATE MULTIPLIERS FOR FPGA APPLICATIONS

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ABSTRACT

It is possible to use a variety of computer arithmetic systems to carry out a complex multiplier. The efficiency of an FPGA-VLSI processor relies on how quickly its digital signal processing operations can be carried out. In order to achieve both high accuracy and speed, the approximation multiplier technique that utilizes compressors and partial product multipliers is proposed. Multiplication is one of the essential functions in all digital systems. Multipliers are generally utilized in digital signal processing and digital image processing applications. Approximate multipliers are widely being used for energy-efficient computing in applications that exhibit an inherent tolerance to inaccuracy. The project is implemented using HDL'S and simulated using Xilinx tools.

INTRODUCTION

The design of high-speed and low-power VLSI architectures need efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption. Adders are the key components in general purpose microprocessors and digital signal processors. They also find use in many other functions such as subtraction, multiplication and division. As a result, it is very pertinent that its performance augers well for their speed performance. Furthermore, for the applications such as the RISC processor design, where single cycle execution of instructions is the key measure of performance of the circuits, use of an efficient adder circuit becomes necessary, to realize efficient system performance. Additionally, the area is an essential factor which is to be taken into account in the design of fast adders. Towards this end, high-speed, low power and area efficient addition and multiplication have always been a fundamental requirement of high-performance processors and systems. The major speed limitation of adders arises from the huge carry

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propagation delay encountered in the conventional adder circuits, such as ripple carry adder and carry save adder.

Power dissipation is one of the most important design objectives in integrated circuit, after speed. Digital signal processing (DSP) circuits whose main building block is a Multiplier-Accumulator (MAC) unit. High speed and low power MAC unit is desirable for any DSP processor. This is because 19 speed and throughput rate are always the concerns of DSP system. Due to rapid growth of portable electronic systems like laptop, calculator, mobile etc., and the low power devices have become very important in today world. Low power and high-throughput circuitry design are playing the challenging role for VLSI designer. For real-time signal processing, a high speed and high throughput MAC unit is always a key to achieve a high performance digital signal processing system. A regular MAC unit consists of multipliers and accumulators that contain the sum of the previous consecutive products. The main motivation of this work is to investigate various multiplier and adder architectures which are suitable for implementing Low power, area efficient and high speed MAC unit.

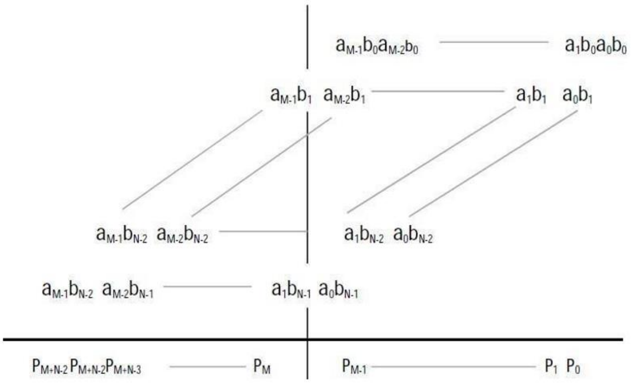
$a_{M-1}b_0a_{M-2}b_0$
$a_1b_0a_0b_0$
$a_{M-1}b_1$ $a_{M-2}b_1$
a_1b_1 a_0b_1
$a_{M-1}b_{N-2}$ $a_{M-2}b_{N-2}$
a_1b_{N-2} a_0b_{N-2}
$a_{M-1}b_{N-2}$ $a_{M-2}b_{N-1}$
a_1b_{N-1} a_0b_{N-1}
$P_{M+N-2}P_{M+N-2}P_{M+N-3}$
P_M
P_{M-1}
P_1 P_0

Figure.1 Partial product array of an M × N multiplier

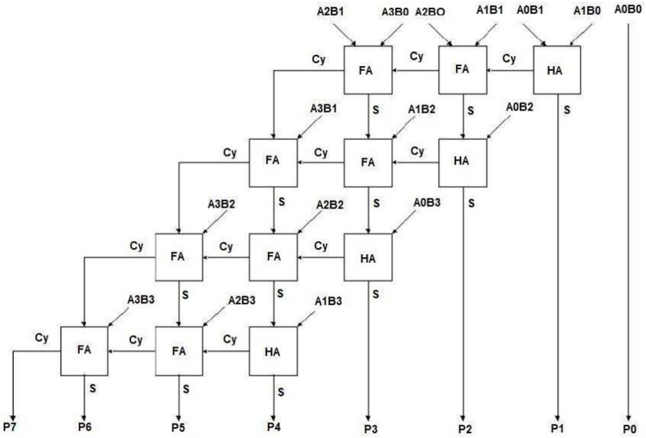

Figure.2 4 Bit Array Multiplier

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LITERATURE SURVEY

1.W. Kamp, A. Bainbridge-Smith, "Multiply Accumulate Unit Optimised for Fast Dot-Product Evaluation", Int. Conf. on Field- Programmable Technology, pp. 349-352, 2007.This literature describes about, A fast dot-product unit suitable for long word lengths is shown. Its implementation is based on computing only the significant partial products and exploiting the properties of the asymmetric signed digit redundant number representation. Optimal partial product packing and a carry propagation free adder combine to yield a MAC with high throughput. An example design of a low-pass FIR filter of 51 taps of 32 bit word-length was synthesised for the Altera cyclone II FPGA family. A filter clock speed of 220 MHz and a throughput of 12.9 MSamples/s was achieved.

2. X. Huang, W. Liu, B. Wei, "A High Performance CMOS Redundant Binary Multiplication-andAccumulation (MAC) Unit", IEEE Trans. Circuits & Syst.-I, Vol. 41 No. 1, pp. 33-44, Jan. 1994. This literature describes about, the design of a pipelined CMOS 16/spl times/16 redundant binary multiplication-and-accumulation (MAC) unit. The MAC unit uses a novel coding scheme for representing binary signed digits. The coding, integrated with the modified Booth algorithm, produces a factor of four reduction in the number of summands feeding the adder tree without preprocessing. The consequent chip layout is compact and small. Furthermore, the MAC's pipeline stages are balanced, resulting in a clock rate exceeding 200 MHz with 0.8-/spl mu/m two-level metal CMOS technology.

3. D. Lee, C. Ryu, K. Kwon, W. Choi, "Design and implementation of 16-bit fixed point digital signal processor", Int. SoC Design Conference, Vol.2 pp 61-64, 2008

This literature describes about, design and implementation of the 16-bit fixed point Digital Signal Processor. The designed DSP has 211 instructions and consists of 40-bit ALU, 6 level pipelines, 17bit X 17-bit parallel multiplier for single-cycle MAC operation, 8 addressing modes, 8 auxiliary registers, 2 auxiliary register arithmetic units, two 40-bit accumulators and 2 address generators. The verilog HDL coded synthesizable RTL code of the DSP core has a complexity of 69,860 in the two input NAND gates. We verified the functions of the DSP by a simulation with a single instruction test as the first step. and then implemented the DSP with the FPGA. The test vectors have a single instruction test, combination of single instructions and algorithm applications, ADPCM vocoder and the MP3 decoder. After FPGA verification, the DSP core is fabricated with 0.25um CMOS technology. The DSP core carried out three test vector sets which are tested at FPGA at the 106 MHz clock rates.

4. A. F. Gonzalez and P. Mazumder, "Redundant Arithmetic: Algorithms and Implementations," INTEGRATION, the International VLSI Journal, Vol. 30, Dec. 2000, pp.13-53.

This literature describes about, Performance in many very-large-scale-integrated (VLSI) systems such as digital signal processing (DSP) chips, is predominantly determined by the speed of arithmetic modules like adders and multipliers. Even though redundant arithmetic algorithms produce signi"cant improvements in performance through the elimination of carry propagation, e$cient circuit implementations of these algorithms have been traditionally di$cult to obtain. This work presents a survey of circuit implementations of redundant arithmetic algorithms. The described implementations are divided into three main groups: (1) conventional binary logic circuits, which encode the multivalued digits of redundant arithmetic into two or more binary digital signals; (2) current-mode multiple-valued logic circuits, which directly represent multivalued redundant digits using non-binary digital current signals; and (3) heterostructure and quantum electronic circuits, intended for very compact designs capable of operating at extremely highspeeds.

5. C. D. Moreno, F. J. Quiles, M. A. Ortiz, M. Brox, J. Hormigo, J. Villababa, E. L. Zapata, "Efficient mapping on FPGA of convolution computation based on combined CSA-CPA Accumulator", Int. Conf. on Electronics, Circuits, and Systems, ICECS 2009, pp. 419-422, 2009. This literature describes about, some architectures to deal with fast convolution computation based on carry save adders which are intended to be specifically implemented on FPGAs. Carry-save adders are not frequent in FPGA implementations since FPGA has a fast carry propagation path. In this paper we prove that it is possible to use carry-save arithmetic in a efficient way on FPGA for convolution operation. We make use of the specific structure of the FPGA to design an optimized accumulator which is able to deal with carry-save additions as well as carry-propagate additions using the same hardware. This lead to an efficient combined CSA-CPA architecture with fast computation and optimizing the hardware cost. Experimental results for different word lengths are presented to validate our proposal.

PROPOSED SYSTEM

The core components of all digital signal processors are the digital multipliers and adders. The speed of the multipliers and adders largely determines the speed of the digital signal processors. The commonly used operation in various Digital signal processing applications

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is the MAC unit. The system performance widely depends on execution time of instruction and the most time consuming process is multiplication.

MAC unit consists of

A multiplier

An accumulator containing the sum of the previous successive products.

The MAC inputs are obtained from the memory location and given to the multiplier block

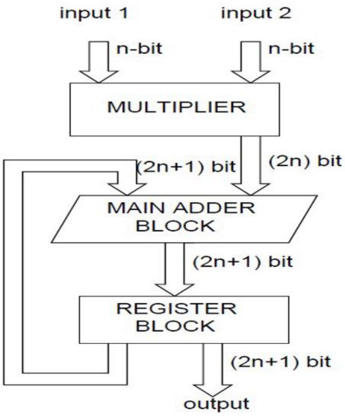

Figure.3 Block Diagram of MAC Unit

Multiplier:

A multiplier can be divided into three steps. The First step is partial product from the multiplier and multiplicand. The Second is adder which adds all the partial products and convert in to the form of sum and carry. The last stage is Final addition in which final multiplication result is generated by adding the sum and carry. for ex.z = a x b + z.

Accumulator:

Accumulator basically consist of register and adder. Register hold the output of the previous clock from adder Holding output in Accumulator register can reduce additional add instruction. An accumulator should be Fast in response so it can be implemented with one of the fastest adders.

Compressors:

Conventionally, 4:2 compressors are used in the multiplier design [1,2]. Fig. 1 (a) gives the block diagram of an accurate (i.e., exact) 4:2 compressor. The four input bits are denoted as X0, X1, X2 and X3. The two output bits in positions i and i+1 are de noted to as Sum and Carry respectively. The carry bit from the lower position is denoted as Cin while the carry bit into the higher position is denoted as Cout

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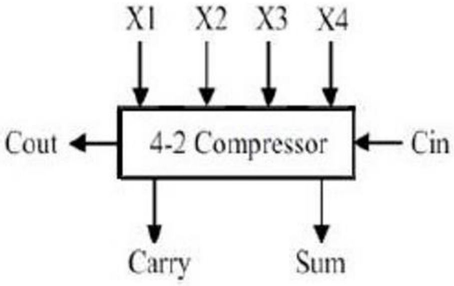
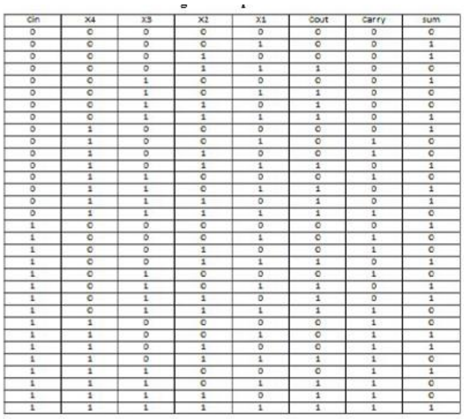


Figure.4 Compressors



Cin	X4	X3	X2	X1	Cout	Carry	sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

Figure.5 Truth table of 4:2 compressor

Bit MAC Using approximate compressors based wallace Multiplier:

The approximate MAC unit using 4:2 compressors in the multiplication process and ripple carry adder is used in the adder block and d flipflop is used for the accumulator for storing the data.

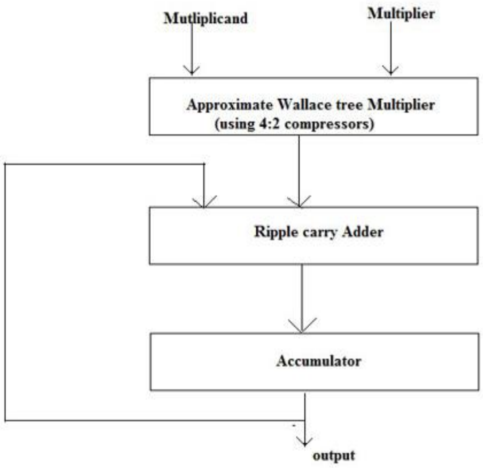


Figure.6 Bit MAC using Approximate compressors

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STIMUALTION RESULTS

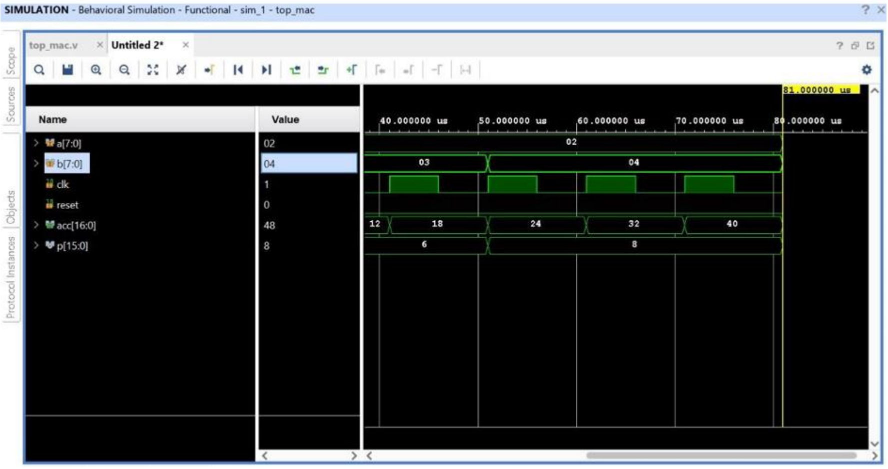


Figure.7 Simulation of MAC Unit

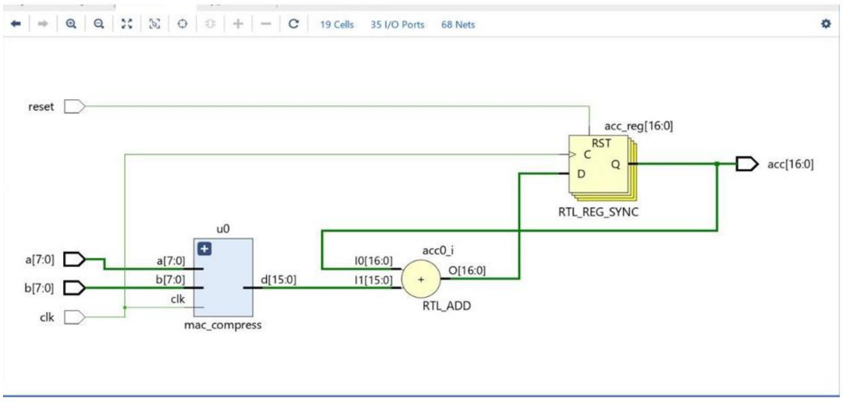


Figure.8 RTL Schematic view of MAC Unit

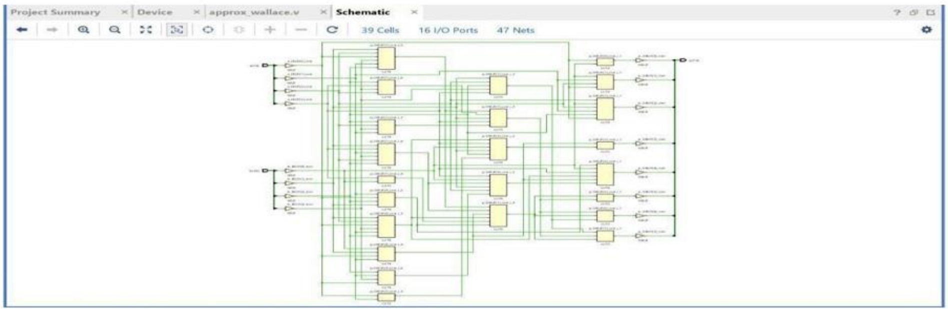
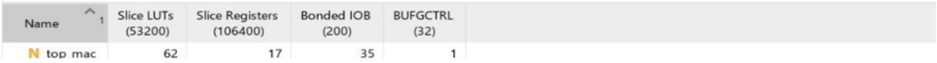


Figure.9 Technology view of MAC Unit



Name	Slice LUTs (53200)	Slice Registers (106400)	Bonded IOB (200)	BUFGCTRL (32)
N top mac	62	17	35	1

Figure.10 Area Utilization Report of MAC Unit

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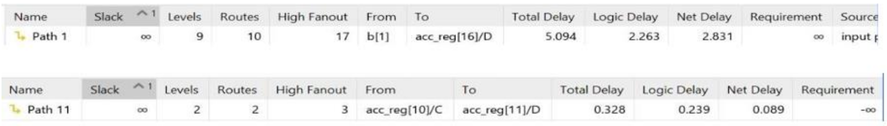
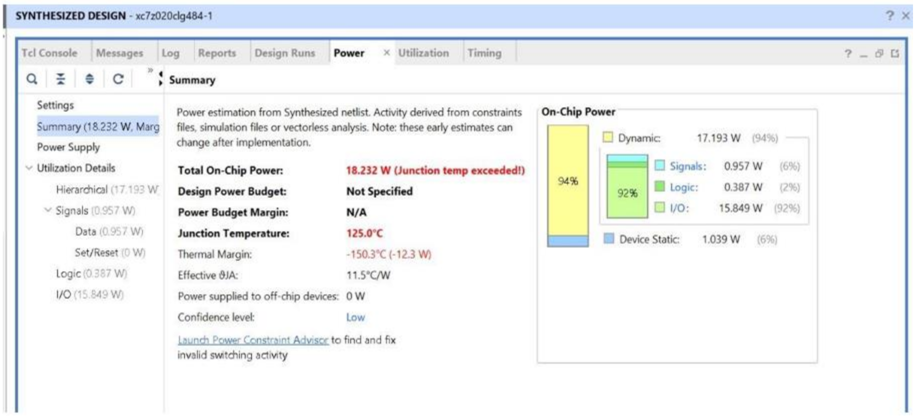


Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	∞	9	10	17	b[1]	acc_reg[16]/D	5.094	2.263	2.831	∞	input p

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 11	∞	2	2	3	acc_reg[10]/C	acc_reg[11]/D	0.328	0.239	0.089	-∞

Figure.11 Hold & Setup Time Delay of MAC Unit



SYNTHESIZED DESIGN - xc7z020clg484-1

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	18.232 W (Junction temp exceeded!)
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	125.0°C
Thermal Margin:	-150.3°C (-12.3 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	17.193 W	(94%)
Signals:	0.957 W	(6%)
Logic:	0.387 W	(2%)
I/O:	15.849 W	(92%)
Device Static:	1.039 W	(6%)

Figure.12 Power Report of MAC Unit

APPLICATIONS

- Digital signal processors.
- Multimedia image processing.
- Image recognition.

ADVANTAGES

- Low Power.
- High speed.

CONCLUSION

Bit MAC unit has been successfully simulated and synthesised using verilog hdl using vivado tool.Different parameters like area, delay, and power reports has been verified for zynq board. Compared with the accurate MAC unit , the proposed MAC unit reduce the area requirement, delay and power consumption by 38%, 46%, and 50%, respectively. In addition, while extending to image processing applications like multiplication, smoothing, and sharpening, the proposed MAC unit attain a better image quality than existing designs, which measure in terms of the mean structural similarity index metric.

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FUTURE SCOPE

Further this bit MAC unit with approximate compressors and this logic can be implemented in image processing for sharpening the images. The efficacy of proposed multipliers in image processing applications such as image multiplication is performed using MATLAB. Based on the achieved results the proposed approximate multipliers are comparable in terms of area, delay, and mean structural similarity index metric (MSSIM) parameter with other works.

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