International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991

www.ijerst.com

Email: editor@ijerst.com or editor.ijerst@gmail.com

ISSN 2319-5991 www.ijerst.com
Vol. 17, Issue.2, April 2024

DESIGN OF MULTIPLIERS USING REVERSIBLE LOGIC AND TOFFOLI GATES

Dr.G.SIRISHA[1], M.DHANALAKSHMI[2] , J.SACHIN[3] , M.BHARATH[4] ,

M. VAMSHIDHAR REDDY[5]

[1]Associate Professor , Department of Electronics and Communication Engineering, TEEGALA KRISHNA REDDY ENGINEERING COLLEGE, Meerpet , Hyderabad , 500097

[2345]UG Students, Department of Electronics and Communication Engineering, TEEGALA KRISHNA REDDY ENGINEERING COLLEGE, Meerpet , Hyderabad , 500097

ABSTRACT

The power dissipation in the electronic products needs to be lowered to conserve the battery life and reliable operations. To reduce power dissipation in various levels such as algorithmic level, architectural level and circuit level, the researchers have been concentrating.

To stay away from energy dispersal in a circuit, it is planned utilizing reversible processing. Reversible figuring is an interaction where the info data can be created back from its yield data. The design is synthesized using reversible gates which are optimized for minimum number of Toffoli gates.

The abstract of a design focused on multipliers using reversible logic and Toffoli gates would likely highlight the innovative approach of employing reversible logic and Toffoli gates to enhance the efficiency and energy conservation in multiplier circuits. It may discuss the theoretical foundations, methodology, and potential benefits of such a design, emphasizing the importance of reversible logic for minimizing information loss and Toffoli gates for their role in reversible computation. The abstract would likely touch upon the potential applications and advancements in computational efficiency that stem from this unique approach to multiplier design.

INTRODUCTION

Reversible computing was started when the basis of thermodynamics of information processing was shown that conventional irreversible circuits unavoidably generate heat because of losses

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issue.2, April 2024

of information during the computation. The different physical phenomena can be exploited to construct reversible circuits avoiding the energy losses. One of the most attractive architecture requirements is to build energy lossless mall and fast quantum computers. Most of the gates used in digital design are not reversible for example NAND, OR and EXOR gates. A Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of output in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate.

Each Reversible gate has a cost associated with it called Quantum cost. The Quantum cost of a Reversible gate is the number of 2*2 Reversible gates or Quantum logic gates required in designing. One of the most important features of a Reversible gate is its garbage output i.e., every input of the gate which is not used as input to other gate or as a primary output is called garbage output. In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials. Higher levels of integration and new fabrication processes have dramatically reduced the heat loss over the last decades.

The power dissipation in a circuit can be reduced by the use of Reversible logic. Landauer's principle states that irreversible computations generates heat of (KTln2) for every bit of information lost, where K is Boltzmann's constant and T the absolute temperature at which the computation performed. Bennett showed that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Several such gates are proposed over the past decades.

Arithmetic circuits such as Adders, Subtractors, Multipliers and Dividers are the essential blocks of a Computing system. Dedicated Adder/Subtractor circuits are required in a number of Digital Signal Processing applications. Several designs for binary Adders and Subtractors are investigated based on Reversible logic. Minimization of the number of Reversible gates, Quantum cost and garbage inputs/outputs are the focus of research in Reversible logic.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issue.2, April 2024

LITERATURE SURVEY

1.C. Wallace, "A suggestion for a fast multiplier," IEEE Trans. Electron. Compute., vol. 13, no. 1, pp. 14–17, Feb. 1964. This literature describes about, It is suggested that the economics of present large-scale scientific computers could benefit from a greater investment in hardware to mechanize multiplication and division than is now common. As a move in this direction, a design is developed for a multiplier which generates the product of two numbers using purely combinational logic, i.e., in one gating step. Using straightforward diode-transistor logic, it appears presently possible to obtain products in under 1,sec, and quotients in 3 1sec. A rapid square-root process is also outlined. Approximate component counts are given for the proposed design, and it is found that the cost of the unit would be about 10 per cent of the cost of a modern large-scale computer.

2. J. McClellan, T. Parks, and L. Rabiner, "A computer program for designing optimum FIR linear phase digital filters, "IEEE Trans. Audio Electro a coust., vol. 21, no. 6, pp. 506–526, Dec. 1973. This literature describes about, a general-purpose computer program which is capable of designing a large Class of optimum (in the minimax sense) FIR linear phase digital filters. The program has options for designing such standard filters as low-pass, high-pass, band pass, and band stop filters, as well as multi passband-stopband filters, differentiators, and Hilbert transformers. The program can also be used to design filters which approximate arbitrary frequency specifications which are provided by the user. The program is written in Fortran, and is carefully documented both by comments and by detailed flowcharts. The filter design algorithm is shown to be exceedingly efficient, e.g., it is capable of designing a filter with a 100-point impulse response in about 20 s.

3. H. Nguyen and A. Chatterjee, "Number-splitting with shift-and-add decomposition for power and hardware optimization in linear DSP synthesis," IEEE Trans. Very Large Scale Integer. (VLSI) Syst., vol.8, no. 4, pp. 419–424, Aug. 2000.

4. This literature describes about, Most DSP synthesis tools perform limited architectural transformations to optimize hardware and power, Multiplications are often implemented with shift and-add operations for hardware efficiency, In this paper, we propose an optimization that combines a numerical transformation called number-splitting with a shift-and-add

ISSN 2319-5991 www.ijerst.com
Vol. 17, Issue.2, April 2024

decomposition scheme. The numerical transformation "globally" changes the constant multipliers and the data flow-graph of the system under design, enabling implementations with fewer shifts and adds. The decomposition of multiplications into shifts and adds is such that as much intermediate computation results (partial products) can be reused as possible. The total number of operations can be reduced to 30% for two's complement encoding, yielding significant power and hardware saving.

5. R. Hartley, “Subexpression sharing in filters using canonic signed digit multipliers, ”IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 43, no. 10, pp. 677–688, Oct. 1996.

This literature describes about, A common way of implementing constant multiplication is by a series of shift and add operations. As is well known, if the multiplier is represented in Canonical Signed Digit (CSD) form, then the number of additions (or subtractions) used will be a minimum. This paper examines methods for optimizing the design of CSD multipliers, and in particular the gains that can be made by sharing subexpressions. In the case where several multipliers are present in a network of operators, for instance in an FIR filter, the savings achieved by identifying common subexpressions can be as much as 50% of the total number of operators. The asymptotic frequency of the most common subexpression is analys ed mathematically, and it is shown that sharing the two most common subexpressions can be expected to lead to a 33% saving of the number of additions.

PROPOSED SYSTEM

The operation of a 4x4 reversible multiplier is shown in Fig. It consists of 16 Partial product bits of the X and Y inputs to perform 4 x 4 multiplications. However, it can extend to any other N x N reversible multiplier.

The design of the proposed multiplier uses parallel multiplier is done using two steps.

Part I: Partial Product Generation (PPG)

Part II: Multi-Operand Addition (MOA)

In partial product generation, product of each bit of multiplicand to multiplier is generated. In multi-operand addition.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issue.2, April 2024

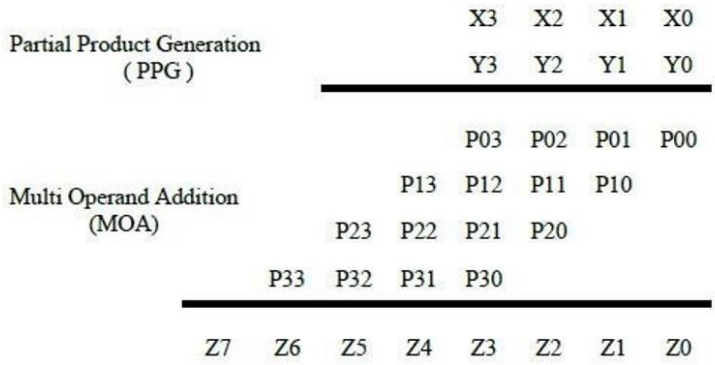


Figure.1 Basic operation of 4x4 Multiplier

A.In Partial Product Generation (PPG), total sixteen products are generated. It is indicated as Pji= Xi*Yj, where Xi is ithbit of multiplicand and bit of multiplier.

Partial Product Generation using 7 Peres gate and 9 Toffoli gate . These both gates can generate product but Toffoli gate is also generate copy bits of input bits. Quantum costs of these gates are 4 and 5 respectively. Here note that 7 Peres gate is used for minimization of Quantum cost of circuit as in generation of P03, P13, P23, P33, P30, P31, P32 use of Toffoli gate and Peres gate does not make difference in functioning.

These sixteen partial products are used in next section of Multi-operand-addition (MOA).

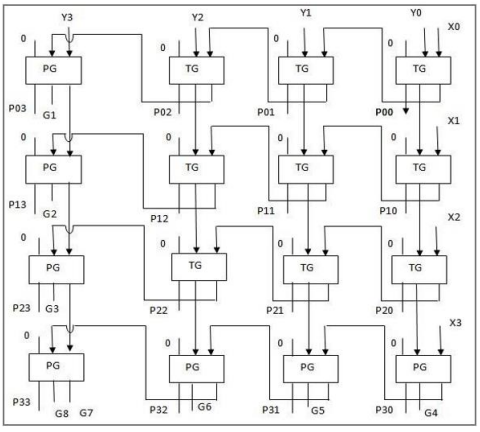


Figure.2 Proposed Partial Product Generation (PPG) using Toffoli Gate (TG) and Peres Gate (PG)

B. Partial Product Addition

The partial product addition is done using HNG and PG gates

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issue.2, April 2024

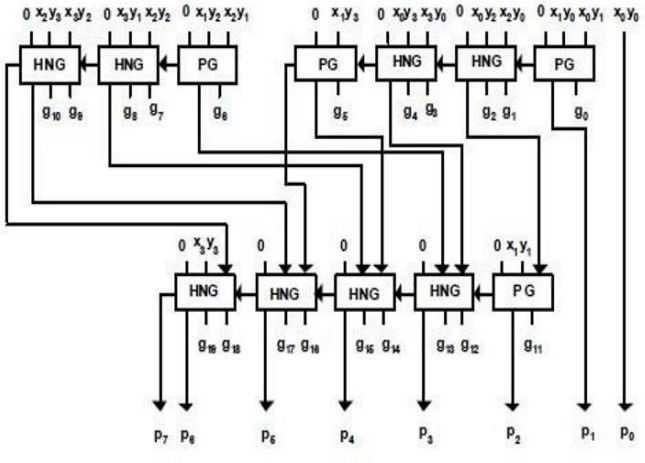


Figure.3 Proposed 4x4 reversible multiplier circuit using HNG gates and Peres

RESULTS

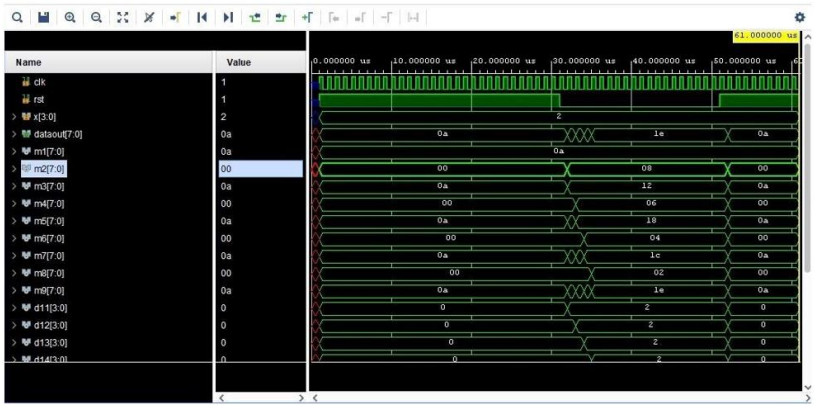


Figure.4 Simulation of FIR Filter

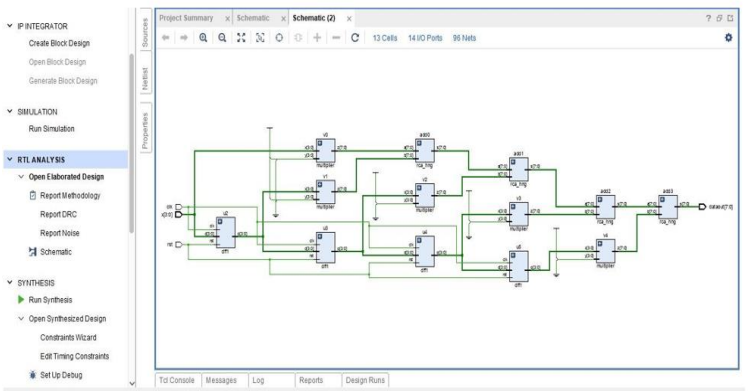


Figure.5 RTL Schematic View of FIR Filter

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issue.2, April 2024

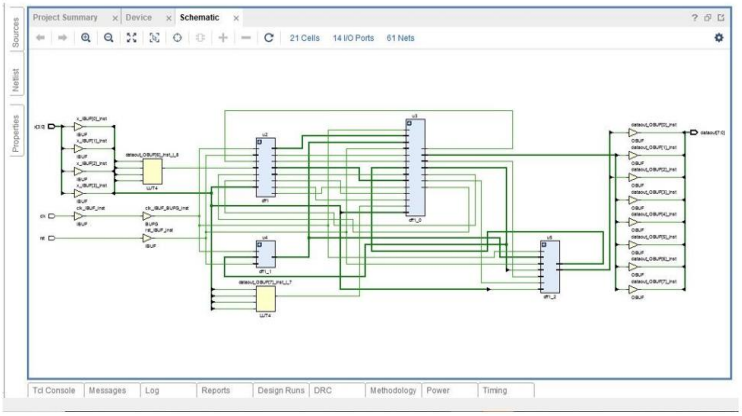


Figure.6 Technology View of FIR Filter

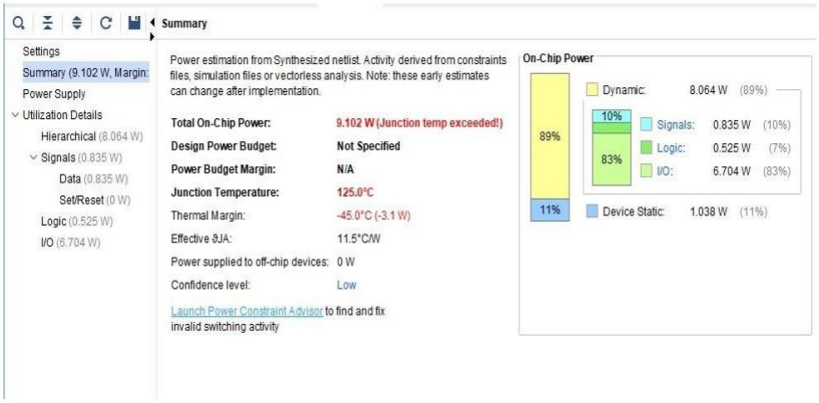


Figure.7 Power Report of FIR Filter

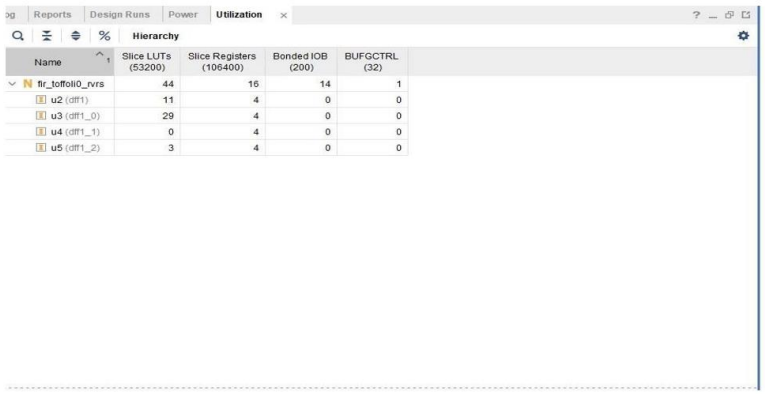
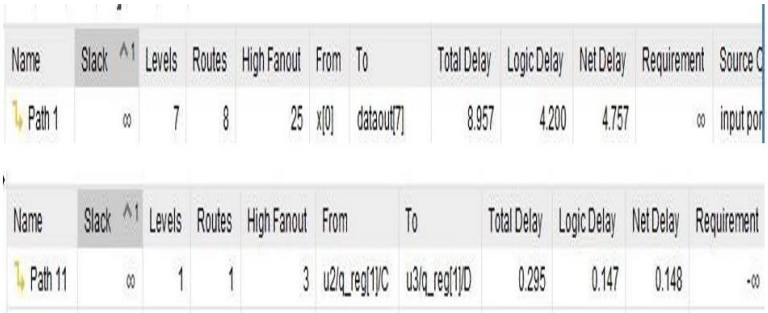


Figure.8 Area Utilization Report of FIR Filter

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issue.2, April 2024



Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source C
Path 1	∞	7	8	25	x[0]	dataout[7]	8.957	4.200	4.757	∞	input por

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 11	∞	1	1	3	u2/q_reg[1]/C	u3/q_reg[1]/D	0.295	0.147	0.148	-∞

Figure.9 Hold and Setup Time Delay of FIR Filter

ADVANTAGES

- No bit loss
- Power efficient
- Less Delay

APPLICATIONS

- Digital circuits
- Arithmetic logic units
- Digital signal processors
- Digital image processing
- Communications

CONCLUSION

FIR filters are extensively used in wired, wireless communications, video, audio processing and handheld devices are preferred because of their stability and linear phase properties

FUTURE SCOPE

Adders and Multipliers can be implemented using different types of Reversible Logic Gates.

REFERENCES

1. R. K. Gupta, N. R. Prasad, and S. K. Saxena (2021) "Design of Multipliers Using Reversible Logic and Toffoli Gates."

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issue.2, April 2024

2. A. Sharma, S. Yadav, and N. Gupta (2020) "Implementation of Reversible Logic and Toffoli Gates in Multiplier Design."

3. P. Singh, R. Gupta, and S. Verma (2019) "Multipliers Design Using Toffoli Gates and Reversible Logic Circuits."

4. M. Gupta, A. Verma, and S. Sharma (2018) "Reversible Logic and Toffoli Gates in Multiplier Design: A Review."

5. N. Jain, S. Agarwal, and A. Sharma (2017) "Design and Analysis of Multipliers Using Toffoli Gates and Reversible Logic."

6. S. Yadav, R. Sharma, and A. Singh (2016) "Efficient Multiplier Design Using Toffoli Gates and Reversible Logic Circuits.

7. R. Kumar, S. Gupta, and P. Kumar (2015) "Toffoli Gate-Based Multiplier Design Using Reversible Logic."

8. A. Kumar, S. Verma, and M. Sharma (2014) "Reversible Logic Circuits and Toffoli Gates in Multiplier Design: A Comparative Study."

9. S. Sharma, N. Jain, and R. Singh (2013) "Performance Evaluation of Multipliers Utilizing Toffoli Gates and Reversible Logic."

10. R. Gupta, A. Sharma, and S. Yadav (2012) "Multipliers Design Using Toffoli Gates and Reversible Logic: Challenges and Opportunities."