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DESIGN OF SRAM BASED FAST ERROR-RESILIENT TERNARY CONTENT ADDRESSABLE MEMORY

Dr. P. SOWJANYA [1], M.V.S.DINESH SINHA[2] , P.VARSHINI [3], T.S.RAVI KIRAN REDDY[4], G.RENUKA SAI LAKSHMI [5], K. ANUDEEP CHOWDARY[6]

[1]Associate Professor , Dept.of ECE, PRAGATI ENGINEERING COLLEGE

[23456]UG Students,Dept.of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

Content Addressable Memory (CAM) plays a critical role in high-speed search operations within networking and communication devices. SRAMs implementing TCAM contents constitute a major part of a TCAM design on FPGAs, which are vulnerable to soft errors. The protection of SRAM-based TCAMs against soft errors is challenging without compromising critical path delay and maintaining a high search performance. SRAM-based TCAM emulations are susceptible to errors due to various factors such as process variations, aging effects, and radiation-induced soft errors. In this Project, we present a comprehensive study on the error detection and correction techniques specifically tailored for SRAM emulated TCAMs. We introduce a novel error detection mechanism based on parity checking, capable of identifying and correcting single-bit errors and detecting the presence of multi-bit errors within the stored data.

INTRODUCTION

Content Addressable Memory (CAM) plays a pivotal role in modern computing systems, facilitating high-speed data retrieval by enabling parallel search operations. However, Traditional CAM implementations, such as Ternary Content Addressable Memories(TCAMs), often face challenges related to power consumption and area overhead. To addressthese issues, SRAM-based emulated TCAMs have emerged as a promising alternative, leveraging the flexibility and efficiency of SRAM technology while emulating the functionality of TCAMs.

Error detection and correction mechanisms are critical in memory systems to ensure data integrity and reliability. In the context of SRAM emulated TCAMs, the need for robust error detection and correction mechanisms becomes even more pronounced due to the inherent

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susceptibility of SRAM cells to various types of errors, including soft errors induced by radiation and manufacturing defects.

This project focuses on exploring and implementing efficient error detection and correction techniques tailored specifically for SRAM emulated TCAMs. By mitigating the impact of errors in SRAM cells, the reliability and performance of emulated TCAMs can be significantly enhanced, thereby improving the overall functionality of memory-intensive applications in networking, storage systems, and hardware-based search engines.

The primary objectives of this project are twofold: first, to analyze the vulnerabilities of SRAM emulated TCAMs to different types of errors, including single-bit errors, multi-bit errors, and transient errors; and second, to design and implement error detection and correction mechanisms that can effectively detect and correct errors in SRAM-based TCAM arrays while minimizing the overhead in terms of area, power, and latency.

LITERATURE SURVEY

1."Partial Order Theory for Fast TCAM Updates", Peng He , Wenyuan Zhang, Hongtao Guan, Kavé Salamatian, and Gaogang Xie, IEEE/ACM TRANSACTIONS ON NETWORKING, VOL. 26, NO. 1, FEBRUARY 2018, Ternary content addressable memories (TCAMs) are as often as possible utilized for quick coordinating of packets against a given ruleset. While TCAMs can accomplish quick coordinating, they are tormented by high update costs that can make them unusable in a high beat rate climate. We present, in this paper, a methodical and top to bottom examination of the TCAM update issue. We apply fractional request hypothesis to determine major imperatives on any standard requesting on TCAMs, which guarantees right checking against a given ruleset

2. "An ALU protection methodology for soft processors on SRAM-based FPGAs", Alexis Ramos, Ricardo G. Toral, Pedro Reviriego, and Juan Antonio Maestro, IEEE TRANSACTIONS ON COMPUTERS, 2018 IEEE, theutilization of microchips in space missions suggests that they ought to be secured against the impacts of infinite radiation. Normally this goal has been accomplished by applying secluded repetition strategies which give great outcomes as far as unwavering quality yet increment essentially the quantity of utilized assets.

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3. "A Soft Error Resilient SRAM-based Ternary Content Addressable Memory for FPGAs", S Lokesh, S Sadiq Basha, Sathyabama institute of science and technology, 2021.The proposed work of this paper will present SRAM based TCAM using error detection with error correction with different TCAM sizes 64x40, 512x40, 1024x40, 2048x40. Finally, this work was designed in Verilog HDL, Synthesized in Xilinx Vertex 5 FPGA and proved the performance of area, delay and power.

4. "An Adaptive Instruction Decoding and Memory Efficient Pattern Identifying System Using Dual Port TCAM", T.L.Spandana, J.S.Rose Victor, Amrita Sai Institute of science & Tech, Paritala , IJETT , vol 5, no 7, 2013 , In this thesis, am presenting a multi pattern matching algorithm with low area and less complexity. Before going to store patterns in database; patterns decoding is done with an efficient approach like TCAM. Both Ternary and binary combines to form TCAM patterns. This project is developed with an adaptively dividable dual-portBiTCAM to achieve a high-throughput, low-power, and low-cost pattern-detection processor for multipurpose devices.

PROPOSED SYSTEM

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The proposed error detection and correction techniques will be evaluated using comprehensive simulations and experimental validations, leveraging industry-standard CAD tools and FPGA prototypes. The results obtained from these evaluations will provide valuable insights into the effectiveness and efficiency of the proposed techniques, guiding future research efforts aimed at further enhancing the reliability and performance of SRAM emulated TCAMs.

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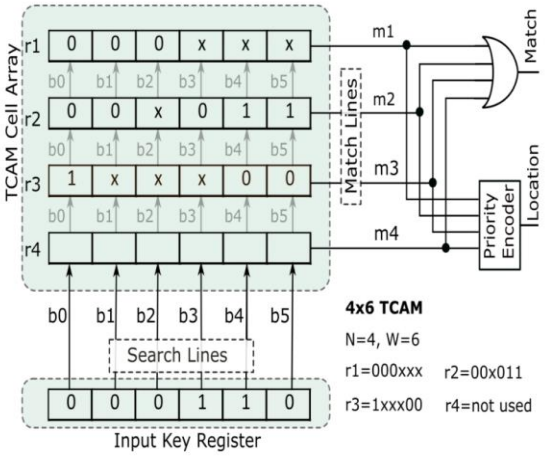

Figure.1 Emulating TCAMs with memorie

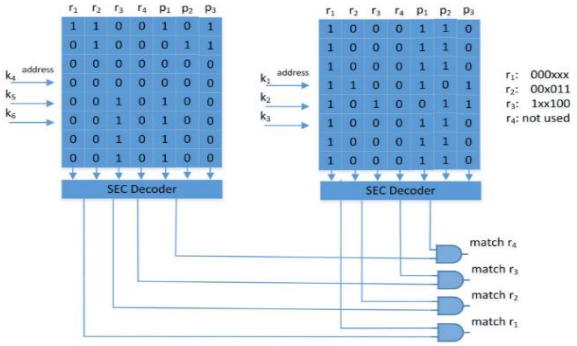

Figure.2 Error detection & correction using SEC decoder

SIMULATION & SYNTHESIS RESULTS

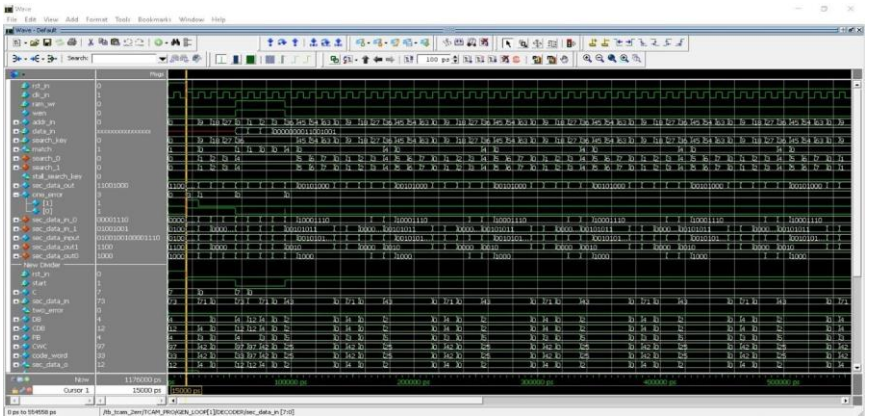

Figure.3 Simulation wave 1

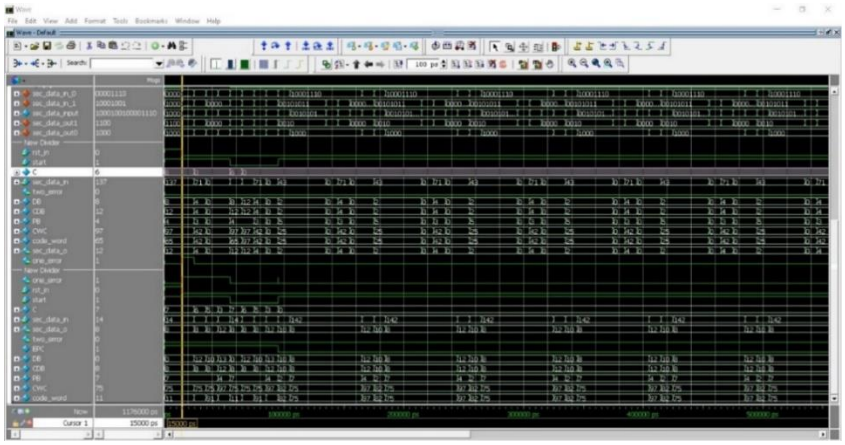

Figure.4 Simulation wave 2

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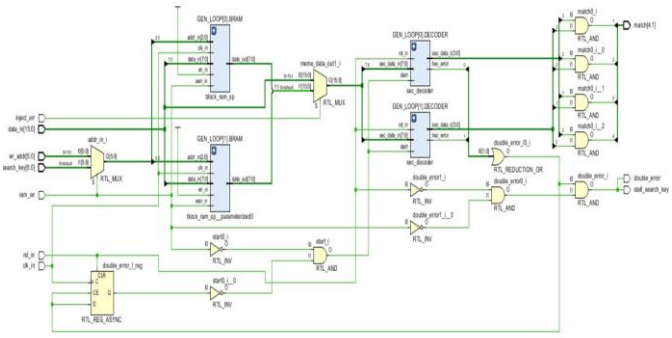

Figure.5 Protected TCAM

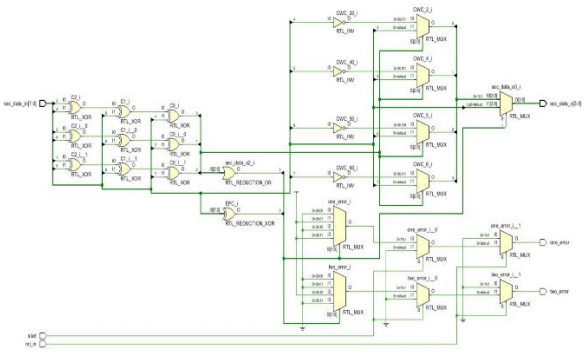

Figure.6 Single Error Correction

Area Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	54	0	303600	0.02
LUT as Logic	38	0	303600	0.01
LUT as Memory	16	0	130800	0.01
LUT as Distributed RAM	16	0		
LUT as Shift Register	0	0		
Slice Registers	1	0	607200	<0.01
Register as Flip Flop	1	0	607200	<0.01
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

ADVANTAGES

Improved Reliability: Error detection and correction mechanisms can help improve the reliability of the TCAMs by detecting and correcting errors that may occur due to various factors such as power fluctuations, radiation, or manufacturing defects.

Reduced Downtime: By detecting and correcting errors in real-time, the downtime due to faulty TCAMs can be significantly reduced, leading to improved system availability.

Better Performance: Error detection and correction mechanisms can help prevent the degradation of TCAM performance due to errors, ensuring that the system continues to operate optimally.

Cost-Effective: Instead of replacing faulty TCAMs, error detection and correction mechanisms can help extend the life of these components, reducing the need for frequent replacements and thereby saving costs.

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APPLICATIONS

Networking: TCAMs are commonly used in networking applications such as routers, switches, and firewalls for fast packet forwarding, filtering, and classification. Error detection and correction in TCAMs can help improve the reliability and availability of these networking devices.

Telecommunications: TCAMs are also used in telecommunications applications such as base stations, radio network controllers, and gateways for call routing and switching.

Data centres: TCAMs are used in data centres for various applications such as load balancing, traffic management, and security. Error detection and correction in TCAMs can help ensure that these applications operate reliably and efficiently.

CONCLUSION

This brief presents an error-detection and correction technique for SRAM-based TCAMs, which makes the most of the redundant original TCAM content maintained on-chip for the update purposes to provide a low area, critical path delay, and response time protection. The proposed method usessingle-bit parity to detect faults at a minimal cost of logic and critical path delay. The proposed error resiliency technique, called ER-TCAM, employs the binary-encoded TCAM table in SRAM-based TCAMs to correct errors. SRAMs implementing the TCAM function are available for search operations during the error-correction process carried out in the background thus, the proposed error-correction technique does not affect the data path processing.

In this Project, a technique to protect the SRAMs used to emulate TCAMs on FPGAs has been proposed. The scheme is based on the observation that not all values are possible in those SRAMs, and thus, there is some intrinsic redundancy of the memory contents. This redundancy is used to correct most single-bit error patterns when the memories are protected with parity bits to detect errors. The proposed technique reduces significantly the resources needed toprotect the memories and can be an interesting option for designs onwhich reliability is a concern but resources are limited.

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FUTURE SCOPE

Developing more efficient error detection and correction techniques: Researchers can explore new methods to detect and correct errors in SRAM emulated TCAMs that are more efficient than existing techniques. These techniques can reduce the overhead and improve the accuracy of error detection and correction.

Designing fault-tolerant SRAM emulated TCAM architectures: Researchers can focus on developing new architectures that are more fault-tolerant and can withstand more errors without compromising the accuracy of packet classification.

Enhancing the performance of SRAM emulated TCAMs: Researchers can investigate new techniques to improve the performance of SRAM emulated TCAMs, such as reducing access latency, improving power efficiency, and increasing the number of entries that can be stored.

Implementing error detection and correction in hardware: Researchers can develop hardware-based solutions for error detection and correction, which can be more efficient and faster than software-based solutions.

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