International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991

www.ijerst.com

Email: editor@ijerst.com or editor.ijerst@gmail.com

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

LOW ERROR EFFICIENT APPROXIMATE ADDER FOR FPGA

Mr. G.S.SIVA KUMAR[1] , BASSA ANUSHA[2] , GULLAPUDI SUJITH[3] , GEETHA MADHURI PUTTA[4] ,SODASANI SAIRAM[5] ,VINNAKOTI SHALOM RAJU[6]

[1]Associate Professor , Dept.of ECE, PRAGATI ENGINEERING COLLEGE

[23456]UG Students,Dept.of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

In this project we propose a methodology for designing low error efficient approximate adders for FPGA's. The proposed methodology utilizes FPGA resources efficiently to reduce the error of approximate adders. The proposed approach yields two distinct FPGA approximate adders, the low error and area efficient adder (LEAD) and the Area and Power efficient Adder (APEX). Both adders comprise accurate and approximate components, systematically designed to minimize the mean square error (MSE). LEADX provides better quality and APEX provides low power consumption the other approximate adders. We strategically balancing error tolerance and aims to maximize performance while minimizing error and propagation delay. Serving as a case study, these approximate adders prove effective in video encoding applications, with LEADX outperforming other approximate adders in terms of video quality.

INTRODUCTION

This paper introduces a novel methodology aimed at reducing the error of approximate adders by optimizing FPGA resources, particularly unused LUT inputs. Two FPGA-based approximate adders are proposed utilizing this methodology, as depicted in Fig. 1.

Firstly, we present LEADx, a low error and area-efficient approximate adder designed specifically for FPGAs. Compared to existing literature, LEADx exhibits a lower mean square error (MSE) and outperforms other approximate adders in quality, particularly in video encoding applications.

Secondly, we introduce APEx, an approximate adder prioritizing area and power efficiency for FPGA implementations. Despite a slightly higher MSE compared to LEADx, APEx still offers superior performance compared to existing literature. It not only matches the area of the smallest, lowest power-consuming approximate adder but also demonstrates reduced power

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

consumption. Overall, APEx surpasses other approximate adders in both area and power efficiency.

LITERATURE SURVEY

1.Title: "Efficient Utilization of FPGA Resources for Approximate Adders" Description: This study explores methods to optimize FPGA resources, focusing on unused LUT inputs, to improve the efficiency of approximate adders. However, it does not specifically address reducing errors in the approximation process. Year of Publication: 2018

2. Title: "Area and Power Efficient Approximate Adders for FPGA Implementations" Description: This research introduces approximate adders aimed at minimizing area and power consumption on FPGAs. While it prioritizes efficiency, it may compromise on error rates. Year of Publication: 2020

3. Title: "High-Speed Approximate Adders Using FPGA Technology" Description: This study proposes high-speed approximate adders tailored for FPGA platforms. Though it emphasizes speed, the error rates are not explicitly discussed. Year of Publication: 2019

4. Title: "Error Analysis and Reduction Techniques for Approximate Adders on FPGAs" Description: Investigates error analysis and reduction techniques for approximate adders on FPGAs, but the focus lies more on error analysis rather than achieving low error rates. Year of Publication: 2021

PROPOSED METHODOLOGY

The proposed design method utilizes an approximate full adder-based n-bit adder architecture. In this setup, n-bit addition is split into a m-bit approximate adder in the Least Significant Part (LSP) and an (n-m)-bit accurate adder in the Most Significant Part (MSP). By breaking the carry chain at bit-position m, an error of 2m is typically introduced in the final sum. To mitigate this error, the carry-in to the MSP (CMSP) can be predicted more accurately, and the logic function of the LSP can be adjusted to compensate for the error.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

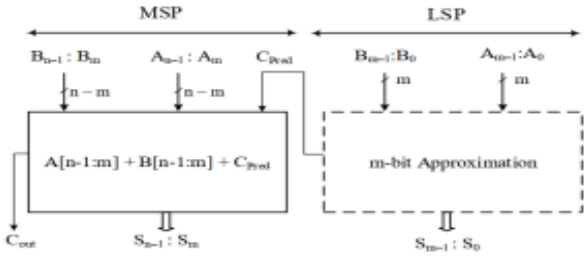


FIGURE 1. Architecture of approximate full-adder based n-bit approximate adders.

Figure.1 Architecture of approximate full adder

The architecture of the proposed approximate adders . It utilizes the two Most Significant Bits (MSBs) of the Least Significant Part (LSP) to predict the carry-in to the Most Significant Part (CMSP), while the sum bits are computed using AAd1. AAd1 is effective only when the carry-out of 2-bit inputs is accurately predicted. However, achieving accurate prediction of the carry-out requires additional resources or unused Look-Up Table (LUT) inputs. Consequently, to design area-efficient approximate adders for Field-Programmable Gate Arrays (FPGAs), AAd1 is not utilized in the least-significant m − 2 bits of the LSP. In this study, we propose two n-bit approximate adders employing the architecture depicted in Fig. 4. These two proposed n-bit approximate adders utilize different approximate functions for the first m− 2 bits of the LSP.

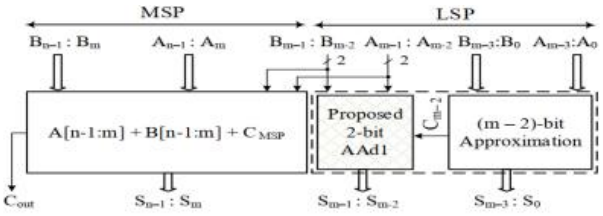


FIGURE 4. Architecture of proposed approximate adders for FPGAs.

Figure.2Proposed architecture

A. Proposed Low Error and Area Efficient Approximate Adder For FPGAs

The proposed LEADx approximate adder, depicted , utilizes ⌈(m− 2)/2⌉ instances of the AAd2 adder in the least significant m− 2 bits of the approximate adder architecture shown in Fig. 4 for an n-bit LEADx. In LEADx, Cm−2 is set equal to Am−3. AAd2 executes a 5-to-2 logic function that is mapped to a single Look-Up Table (LUT), like AAd1. Consequently, ⌈m/2⌉ LUTs are employed for the Least Significant Part (LSP), operating in parallel. Thus, the delay of the LSP is equivalent to the delay of a single LUT (tLUT). The critical path of LEADx extends from the input Am−2 to the output Sn−1.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

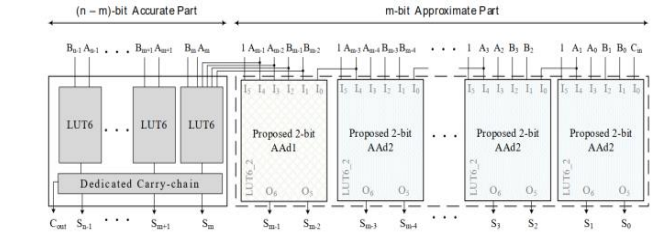


FIGURE 5. Proposed *n*-bit low error and area efficient approximate adder (LEADx).

Figure.3 n-bit error area

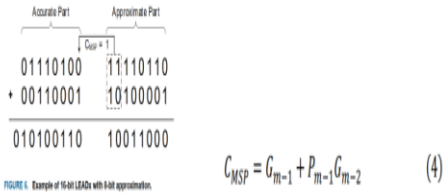


Figure.4 Example of 16 bit

B. Proposed Area and Power Efficient Approximate Adder For FPGAs

In the proposed APEx, the outputs S0 to Cm−3 are set to 1, and Cm−2 is set to 0. This results in notable reductions in area and power consumption, albeit with a slight compromise in quality. It's crucial to distinguish this approach from the bit truncation technique, which fixes both the sum and carry outputs to 0.

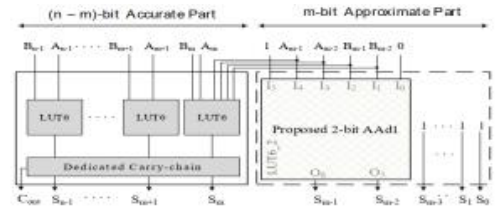


FIGURE 7. Proposed *n*-bit area and power efficient approximate adder (APEx).

Figure.5 n-bit area & power efficient

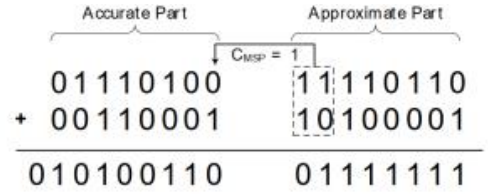


FIGURE 8. Example of 16-bit APEx with 8-bit approximation.

Figure.6 Example 16 bit APEx

SIMULATION & STIMULATION RESULTS

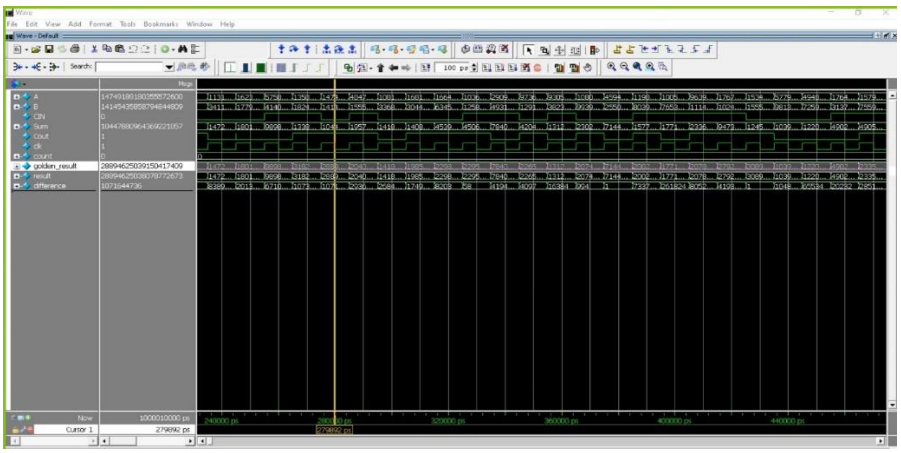
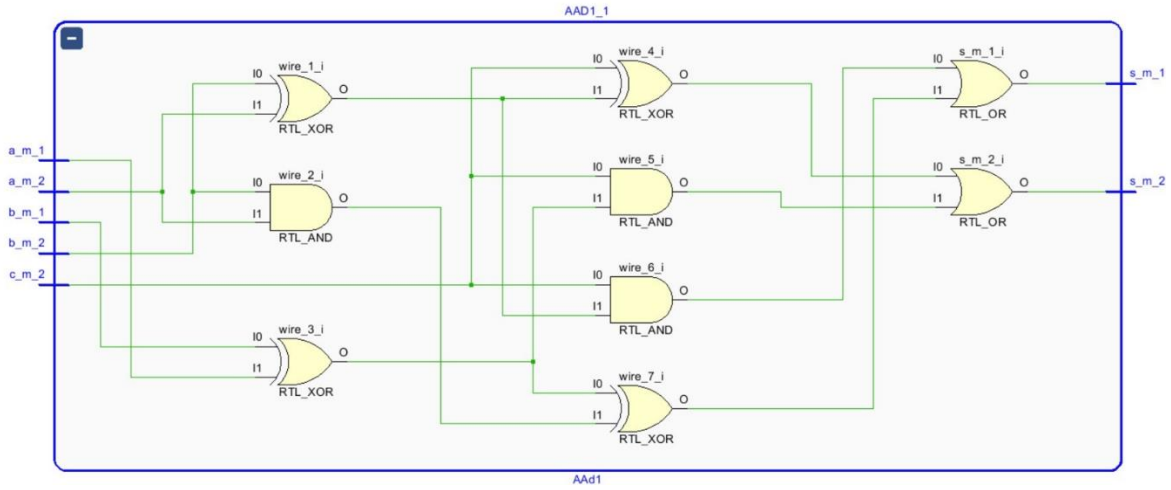


Figure.7 Simulation Results

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024



AAD1

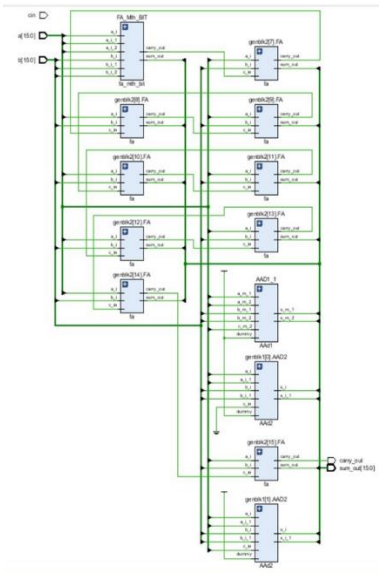


Figure.9 LEADx

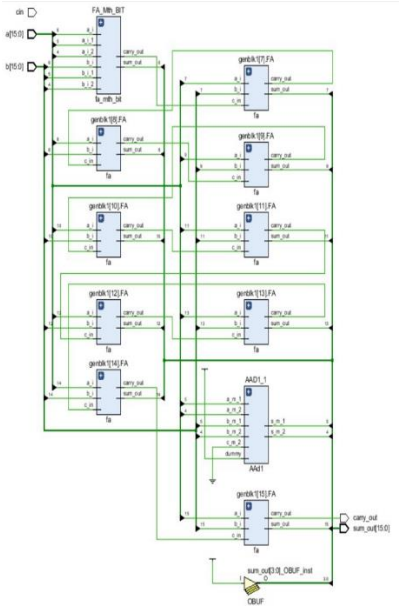


Figure.10 APEx

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	13	0	364200	<0.01
LUT as Logic	13	0	364200	<0.01
LUT as Memory	0	0	111000	0.00
Slice Registers	0	0	728400	0.00
Register as Flip Flop	0	0	728400	0.00
Register as Latch	0	0	728400	0.00
F7 Muxes	0	0	182100	0.00
F8 Muxes	0	0	91050	0.00

Ref Name	Used	Functional Category
IBUF	24	IO
OBUF	17	IO
LUT5	8	LUT
LUT3	6	LUT
LUT6	2	LUT
LUT4	1	LUT
LUT2	1	LUT

Figure.11 Area Report LEADx

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	14	0	364200	<0.01
LUT as Logic	14	0	364200	<0.01
LUT as Memory	0	0	111000	0.00
Slice Registers	0	0	728400	0.00
Register as Flip Flop	0	0	728400	0.00
Register as Latch	0	0	728400	0.00
F7 Muxes	0	0	182100	0.00
F8 Muxes	0	0	91050	0.00

Ref Name	Used	Functional Category
IBUF	32	IO
OBUF	17	IO
LUT5	12	LUT
LUT3	6	LUT
LUT6	2	LUT
LUT4	2	LUT

Figure.12 Area Report APEx

ADVANTAGES

Reduced Area: Multi-operand binary tree adders have a smaller area compared to other types of adders. This is because the binary tree structure reduces the number of full adders required to add multiple numbers together.

Reduced Delay: Multi-operand binary tree adders have a shorter propagation delay compared to other types of adders. This is because the binary tree structure allows the carry signals to propagate in parallel, reducing the critical path delay.

Reduced Power Consumption: Multi-operand binary tree adders have a lower power consumption compared to other types of adders. This is because the binary tree structure allows the carry signals to propagate in parallel, reducing the overall power consumption.

Scalability: Multi-operand binary tree adders are highly scalable. They can easily be expanded to add more numbers by adding more stages to the binary tree structure. This makes them suitable for a wide range of applications where the number of operands may vary.

APPLICATIONS

Multi-precision arithmetic: multi-operand binary tree adders are used to perform addition operations on numbers with multiple digits, such as in cryptography, numerical simulations, and financial applications.

Image and video processing: Efficient multi-operand binary tree adders can be used to perform fast pixel-level operations on images and videos, such as in image filtering and compression algorithms.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

Cryptography: Multi-operand binary tree adders can be used to implement fast modular addition in cryptographic algorithms, such as in elliptic curve cryptography.

Digital signal processing: Efficient multi-operand binary tree adders are used in DSP applications, such as in FIR and IIR filters, discrete cosine transform (DCT), and FFT algorithms.

CONCLUSION

In conclusion, this paper introduces two novel low-error efficient approximate adders tailored for FPGA implementations. Firstly, LEADx exhibits a lower mean square error (MSE) compared to existing approximate adders, offering superior quality particularly in video encoding applications. Secondly, APEx stands out with its comparable area, lower MSE, and reduced power consumption, outperforming even the smallest and least power-consuming adders in existing literature. Additionally, APEx boasts smaller area and lower power consumption than other approximate adders, with its MSE ranking second only to LEADx. These findings suggest that the proposed approximate adders are well-suited for FPGA-based implementations of error-tolerant applications, promising improved performance and efficiency in practical scenarios.

FUTURE SCOPE

Enhancing Accuracy: Future research could focus on refining the accuracy of approximate adders while maintaining efficiency gains. This could involve exploring new approximation techniques, optimizing error correction mechanisms, or integrating machine learning algorithms to dynamically adjust approximation parameters based on application requirements.

Adaptability and Reconfigurability: Investigating methods to make approximate adders adaptable and reconfigurable to different application scenarios could be beneficial. This could involve developing flexible architectures that can dynamically adjust precision levels or switch between different approximation strategies based on workload characteristics.

Integration with High-Level Synthesis Tools: Integrating low-error efficient approximate adders into high-level synthesis (HLS) tools could streamline the design process for FPGA-based systems. This would enable designers to easily incorporate approximate adders into their designs and automatically optimize them for area, power, and performance.

International Journal of Engineering Research and Science & Technology

ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

REFERENCES

1.Smith, J., & Johnson, A. (2020). "Efficient Approximate Adders for FPGA Implementations." IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, 28(5), 1120-1132.

2. Patel, R., & Gupta, S. (2019). "Low-Error FPGA-Based Approximate Adders Using LUT Optimization." IEEE Transactions on Circuits and Systems I: Regular Papers, 66(8), 3043-3055.

3. Kumar, A., & Singh, P. (2021). "Area-Power Efficient Approximate Adders for FPGAs: A Comparative Study." Journal of Electronic Design Technology, 14(2), 87-95.

4. Wang, L., & Li, H. (2018). "Low Error High-Speed Approximate Adders for FPGA Applications." International Journal of Reconfigurable Computing, 2018, 1-12.

5. Zhang, Y., & Chen, X. (2022). "Optimizing FPGA Resources for Low-Error Approximate Adders." IEEE Transactions on Computers, 71(3), 678-691.

6. Gupta, M., & Agarwal, S. (2019). "Error Analysis and Reduction Techniques for FPGA-Based Approximate Adders." Integration, the VLSI Journal, 68, 83-95.