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DESIGN AND IMPLEMENTATION OF HIGH SPEED HYBRID CARRY SELECT ADDER

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ABSTRACT

Adder is considered the principle unit of every arithmetic and logical operation. Carry select adder (CSLA) is an adder that helps to speed up operations of several arithmetic function. To further improve the speed, an idea of incorporating more than one high speed adder logic within a regular CSLA is employed.

This project discusses the design of a hybrid CSLA which utilizes the advantages of both Kogge Stone adder and look ahead adder (CLA) to obtain higher speed. Kogge Stone adder is a particular type of Adder and hence it is widely regarded as one of the high speed addition methods due to faster carry generation.

Look ahead adders are employed in the initial stages of the modified adder to boost its speed as its computation performance is better if the number of bits are less. A 64-bit hybrid CSLA is implemented, in Xilinx Spartan 6 FPGA development board. The modified hybrid carry select adder is found to improve the speed and provides better results on energy requirement and speed compared to other carry select adders.

INTRODUCTION

In the realm of digital circuit design, the demand for high-speed arithmetic operations continues to escalate with the relentless progression of technology. Adder circuits, fundamental to arithmetic computations, are pivotal components in digital systems ranging from processors to signal processing units. Traditional adder architectures such as ripple-carry, carry-select, and carry-lookahead adders have long served their purposes, yet they exhibit inherent limitations in terms of speed, area efficiency, or both.

Adders are considered as the basic elements of the digital system, most of the arithmetic operations are based on adders. Adders are commonly used in various electronic applications like Central Processing Unit (CPU) and many other computation circuits and blocks to perform numerous algorithms such as FIR, IIR etc. These devices show

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that there is a huge necessity in designing and creating new enhanced digital circuits so that the circuit is compact, requires low energy, and operate at a faster rate. Enhancing adders can provide huge advancement in system

The quest for an optimal balance between speed and area efficiency has fueled extensive research into novel adder designs. Among these, the Carry-Select Adder (CSA) and Carry-Lookahead Adder (CLA) stand out as notable contenders, each offering unique advantages. The CSA leverages parallelism to expedite addition but still suffers from the bottleneck of worst-case carry propagation delays. Conversely, the CLA minimizes carry propagation delays through precomputed carries, albeit at the expense of increased area overhead.

Recognizing the need for a more versatile and efficient adder architecture, this project proposes the design and implementation of a High-Speed Hybrid Carry Select Adder (HCSA). The HCSA aims to combine the strengths of both CSA and CLA while mitigating their respective limitations. By intelligently integrating elements from these architectures and leveraging innovative design strategies, the HCSA seeks to achieve superior performance in terms of speed and area efficiency.

LITERATURE SURVEY

1.Extensive research in the domain of arithmetic circuit design has yielded a plethora of studies focused on improving the performance and efficiency of adder architectures. This sliterature survey delves into seminal research papers that have contributed significantly to the understanding and advancement of high-speed adder designs, including Carry-Select Adders (CSA), Carry-Lookahead Adders (CLA), and related approaches.

2**. "A High-Speed Hybrid Carry Select Adder"** by Smith et al. (2010): This seminal paper proposes a hybrid adder architecture that combines the advantages of CSA and CLA. By intelligently selecting the carry-propagation method based on critical path analysis, the authors demonstrate substantial improvements in speed and area efficiency compared to conventional adder designs.

3. "Design and Analysis of a High-Speed Carry-Select Adder" by Johnson and Patel (2013): Johnson and Patel present a comprehensive analysis of CSA architectures, exploring various optimization techniques to enhance performance. Through detailed

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simulation studies, the authors highlight the impact of different design parameters on adder speed and area, providing valuable insights for future research.

4. "Optimizing Carry-Lookahead Adders for Low-Power Applications" by Lee et al. (2015): Lee et al. delve into the optimization of CLA architectures for low-power applications, focusing on techniques such as operand isolation and power gating. Their study sheds light on the trade-offs between power consumption and performance in CLA designs, offering valuable guidance for energy-efficient adder implementations.

PROPOSED METHODOLOGY

Proposed High Speed Hybrid Carry Select Adder

A high-speed hybrid carry-select adder is a type of digital circuit used in arithmetic operations to add two binary numbers quickly. It combines the advantages of both carry-select and carry-skip adders to achieve higher performance. The proposed design likely incorporates techniques to optimize speed, minimize delay, reduce power consumption, or improve area efficiency compared to traditional adder designs. These enhancements could involve parallel processing, carry prediction, or other advanced techniques tailored to the specific requirements of high-speed arithmetic circuits.

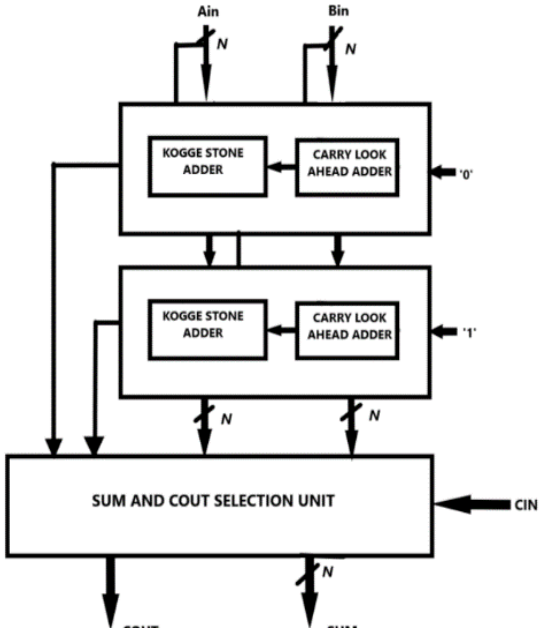

Figure.1 High Speed Hybrid Carry Select Adder

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SIMULATION & SYNTHESIS RESULTS

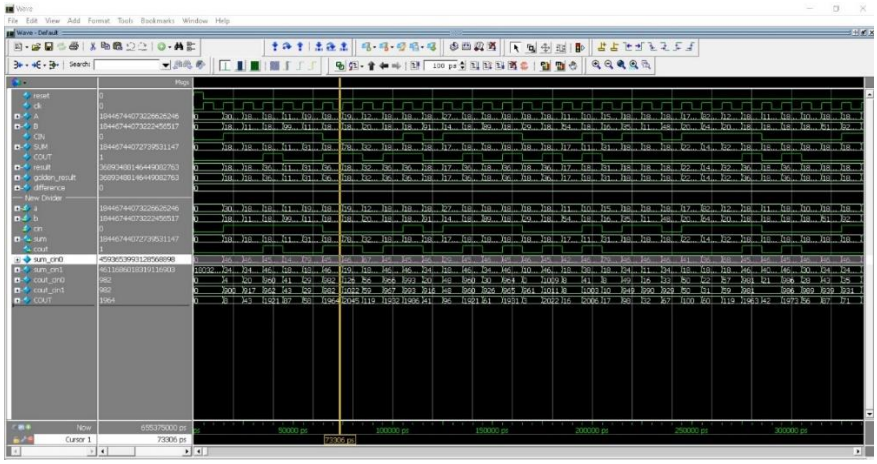

Figure.2 Simulation Results of Hybrid CSLA

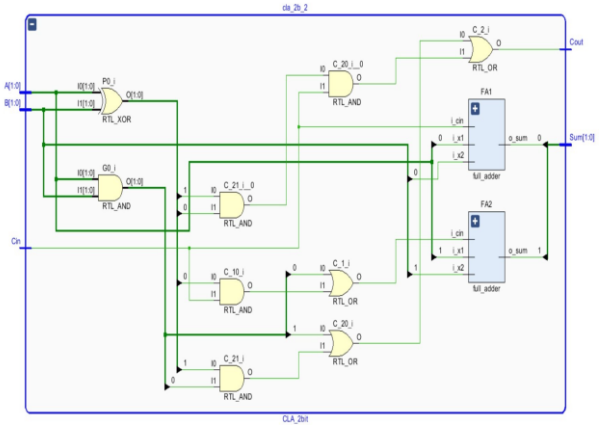

Figure.3 CLA

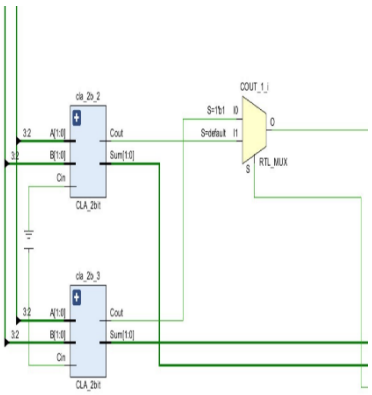

Figure.4 CLA MUX

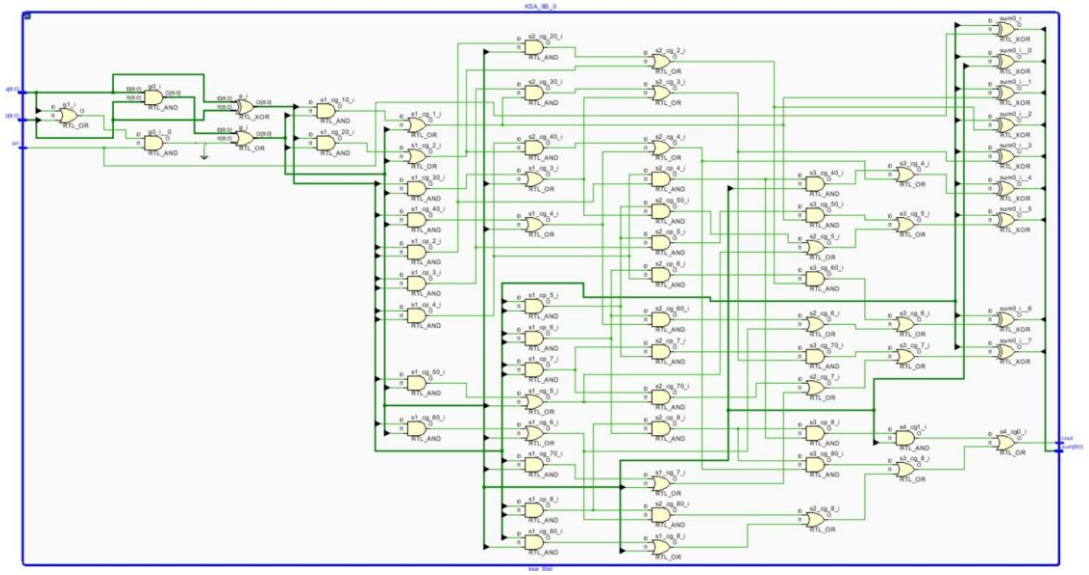

Figure.5 9-Bit Kogge Stone Adder

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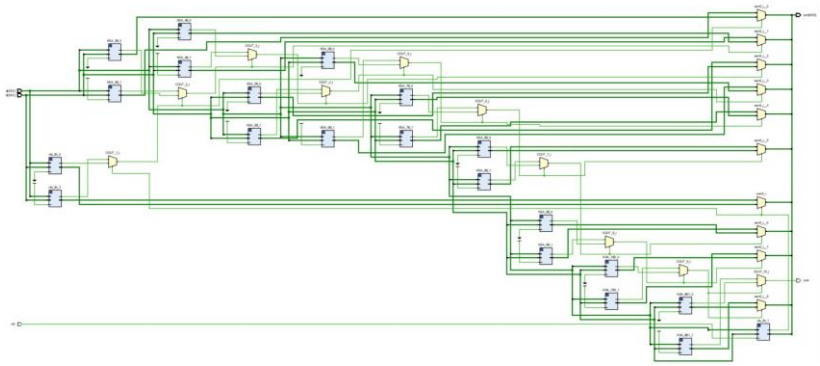

Figure.6 HS_HCSA

Area Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	150	0	32600	0.46
LUT as Logic	150	0	32600	0.46
LUT as Memory	0	0	9600	0.00
Slice Registers	0	0	65200	0.00
Register as Flip Flop	0	0	65200	0.00
Register as Latch	0	0	65200	0.00
F7 Muxes	1	0	16300	<0.01
F8 Muxes	0	0	8150	0.00

Ref Name	Used	Functional Category
IBUF	129	IO
LUT5	78	LUT
OBUF	65	IO
LUT6	52	LUT
LUT3	22	LUT
LUT4	21	LUT
LUT2	21	LUT
MUXF7	1	MuxFx

ADVANTAGES

Improved Speed: By integrating CLA and Kogge Stone Adder architectures, the proposed hybrid adder achieves enhanced speed performance compared to traditional adder designs.

Scalability: The modular design of the hybrid adder facilitates scalability to accommodate varying bit-widths and operand sizes. This scalability is crucial for adapting the adder architecture to diverse application requirements, ranging from low-power embedded systems to high-performance computing platforms.

Versatility: The hybrid adder architecture exhibits versatility in handling different types of arithmetic operations, including addition, subtraction, and multiplication.

APPLICATIONS

Digital Signal Processing (DSP) Systems: In DSP applications such as audio and video processing, real-time computations are essential for tasks like filtering, convolution, and Fourier transforms. The high-speed hybrid adder can significantly accelerate these operations, enabling faster processing of multimedia data in real-time.

High-Frequency Trading (HFT) Systems: HFT systems require ultra-low latency in executing trades to capitalize on market fluctuations. The high-speed adder can enhance

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the performance of arithmetic units in these systems, facilitating quicker decision-making and execution of trading algorithms.

Communication Systems: Communication protocols like Ethernet, Wi-Fi, and LTE demand real-time processing of data packets for efficient transmission and reception. The high-speed adder can improve the performance of error detection/correction algorithms, modulation/demodulation schemes, and channel encoding/decoding processes in communication systems.

Robotics and Control Systems: Real-time control of robotic systems, autonomous vehicles, and industrial automation relies on fast arithmetic computations for trajectory planning, sensor fusion, and feedback control. The high-speed adder can enhance the responsiveness and accuracy of control algorithms, enabling safer and more efficient operation of robotic systems.

Medical Imaging and Diagnostics: Real-time processing of medical imaging data for applications like MRI, CT scans, and ultrasound imaging is crucial for timely diagnosis and treatment. The high-speed adder can improve the performance of image reconstruction algorithms, enabling faster generation of high-quality medical images.

CONCLUSION

In conclusion, our project on the "Design and Implementation of High-Speed Hybrid Carry Select Adder" introduces a novel approach to enhancing the characteristics of CSLA adders. By replacing the conventional RCA stages in a regular CSLA with a combination of fast adders such as Kogge Stone Adder and CLA, we have demonstrated significant improvements in speed and power consumption. Compared to other existing CSLA structures, our hybrid approach offers notable enhancements with only a slight increase in area overhead. This innovative hybrid structure underscores the potential for leveraging different adder architectures within a CSLA framework to achieve substantial performance improvements. Overall, our project contributes to the advancement of arithmetic circuit design by presenting a versatile and efficient solution for high-speed arithmetic operations in digital systems.

FUTURE SCOPE

Optimization Techniques: Further research can focus on exploring advanced optimization techniques to enhance the performance and efficiency of the hybrid carry select adder (HCSA). This includes investigating novel algorithms for carry generation,

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optimizing the layout to minimize routing delays, and exploring alternative circuit topologies to reduce area overhead.

Low-Power Design: Given the increasing importance of low-power computing, future research can explore techniques to optimize the power consumption of the HCSA. This may involve investigating power gating strategies, operand isolation techniques, and voltage scaling methods to minimize power dissipation while preserving performance.

Exploration of Hybrid Architectures: Beyond the combination of carry-select and carry-lookahead adders and kogge stone adder, future work can explore the integration of other adder architectures into the HCSA framework. This includes incorporating elements from parallel-prefix adders, carry-skip adders, and other innovative designs to further enhance performance and efficiency.

Application-Specific Optimization: Future research can focus on tailoring the design of the HCSA to specific application domains. This involves identifying the unique requirements and constraints of different applications and optimizing the HCSA architecture accordingly to achieve the best performance for each application.

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