International Journal of Engineering Research and Science & Technology

IJERST

ISSN : 2319-5991

www.ijerst.com

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International Journal of Engineering Research and Science & Technology
ISSN 2319-5991 www.ijerst.com
Vol. 17, Issuse.1, March 2024

EFFICIENT IMPLEMENTATION OF 2,4,8 BIT MULTIPLIERSWITH "URDHAVA TRIYAKBHYAM" VEDIC ALGORITHM

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ABSTRACT

This Project presents a VLSI implementation of a Vedic multiplier utilizing the Urdhva–Tiryakbhyam Sutra, a traditional Indian mathematical technique, within a Verilog environment. The proposed design leverages the sutra's unique mathematical principlesto achieve efficient and high-speed multiplication.

The Verilog implementation ensures a seamless integration into digital circuits. The utilization of VLSI technology enhances the overall performance, making the multiplier suitable for modern computational applications. We are designing 2x2,4x4 and 8x8 multipliers. The results demonstrate the effectiveness of the Vedic multiplier in terms ofspeed and resource utilization, establishing its relevance in modern digital systems.

INTRODUCTION

In the realm of digital circuit design, the quest for more efficient and faster arithmetic units has been a perennial pursuit. Multiplication, being one of the fundamental operations in digital computing, plays a pivotal role in various applications ranging from signal processing to cryptographic algorithms. In this context, the exploration of novel multiplication algorithms and their efficient VLSI implementations holds immense significance.

This project endeavours to explore the application of the ancient Vedic multiplication technique known as "Urdhava Triyakbhyam" in the design and implementation of 2, 4, and 8-bit multipliers. The Vedic system of mathematics, originating from ancient Indiantexts like the Vedas, offers alternative methods for arithmetic operations that are often characterized by their simplicity and efficiency.

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The "Urdhava Triyakbhyam" algorithm, which translates to "Vertically and Crosswise,"presents a unique approach to multiplication that exploits the principles of digit-by-digitmultiplication and summation to achieve results efficiently. By leveraging this ancient algorithm, we aim to develop VLSI implementations of 2, 4, and 8-bit multipliers that offer improved performance in terms of speed, area efficiency, and power consumption compared to conventional multiplication techniques.

OBJECTIVE

The objective of this project is to achieve an efficient VLSI implementation of 2, 4, and 8-bit multipliers using the "Urdhava Triyakbhyam" Vedic algorithm. The primary focus is on optimizing the performance of the multipliers by leveraging the mathematical principles embedded in the Vedic algorithm. The goal is to design a VLSI architecture that maximizes speed, minimizes power consumption, and occupies minimal chip area.

LITERATURE SURVEY

1.Paper Title: **"Efficient Implementation of 8x8 Bit Multiplier using Urdhva Tiryagbhyam"**

Authors: Vijaykumar N, Lokesh B.G, Sachin G. T and Dr. Shilpa G. S Year of Publication: 2016

Disadvantages: While this paper focuses on the efficient implementation of an 8x8 bit multiplier using the Urdhva Tiryagbhyam algorithm, it may not delve deeply into the challenges and limitations of scaling the algorithm for 2-bit and4-bit multipliers. Additionally, it might not address the trade-offs involved in implementing the algorithm in VLSI due to area, power, and speed constraints.

2. Paper Title: **"Design and Implementation of Low Power Vedic Multiplier UsingParallel Prefix Adders"**

Authors: Anshika Sharma, Tarun Kumar Gupta Year of Publication: 2020

Disadvantages: While this paper discusses the design and implementation of alow-power Vedic multiplier, it may not specifically focus on the "Urdhva Triyakbhyam" algorithm or its application in 2-bit and 4-bit multipliers. Therefore, it may not provide detailed insights into the specific challenges andoptimizations required for efficiently implementing the algorithm in VLSI circuits.

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3. Paper Title: **"Design of High Speed 4-Bit Multiplier Based on Vedic Mathematics"**

Authors: M. A. Javeed, Y. V. Subba Rao, K. V. V. Satyanarayana Year of Publication: 2018

Disadvantages: Although this paper presents a high-speed 4-bit multiplier based on Vedic Mathematics principles, it may not thoroughly explore the "Urdhva Triyakbhyam" algorithm or its implementation challenges. Moreover,it may not address the trade-offs between speed, area, and power consumptionin VLSI implementation.

PROPOSED METHODOLOGY

The proposed methodology for the efficient VLSI implementation of 2, 4, and 8-bit multipliers with the "Urdhava Triyakbhyam" Vedic algorithm involves a series of key steps aimed at outperforming existing methodologies.

Firstly, a thorough understanding and analysis of the Urdhava Triyakbhyam algorithm will be conducted to identify its inherent parallelism and mathematicalproperties. This understanding will guide the design process to leverage the algorithm's strengths for efficient multiplication.

Next, a novel architecture will be developed that optimally exploits the parallelprocessing capabilities of the algorithm, reducing critical path delays. The design will prioritize the minimization of power consumption and chip area occupation while maximizing computational speed.

Advanced simulation and verification techniques will be employed to ensure theaccuracy and reliability of the proposed design. This will involve rigorous testing against a variety of input scenarios to validate the performance and correctness of the multiplier.

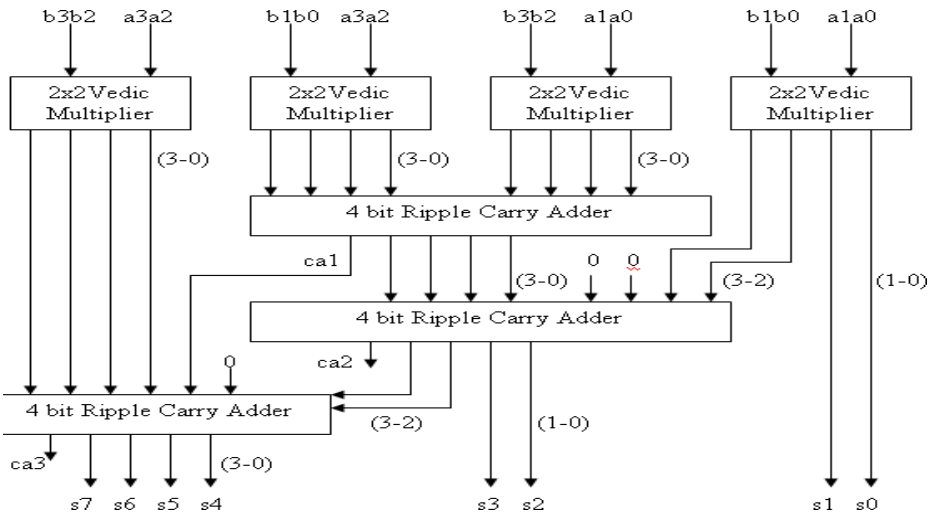

Figure.1 Block Diagram of 4x4 bit Vedic Multiplier

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ISSN 2319-5991 www.ijerst.com

Vol. 17, Issuse.1, March 2024

SIMULATION & SYNTHESIS RESULTS

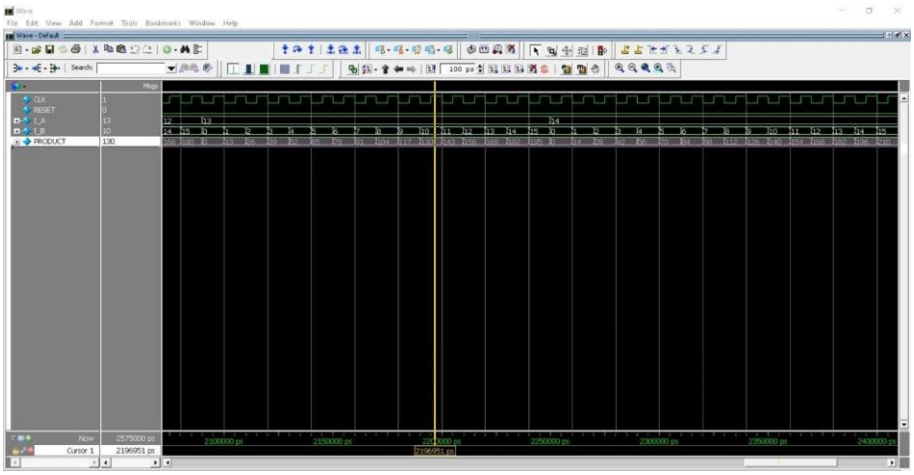

Figure.2 Simulation Results of 4-bit Multiplier using Vedic Algorithm

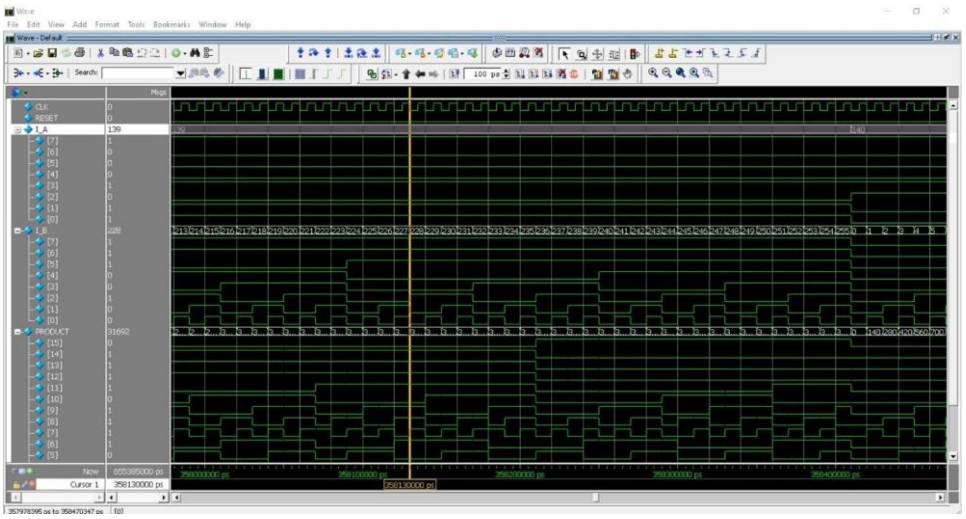

Figure.3 Simulation Results of 8-bit Multiplier using Vedic Algorithm

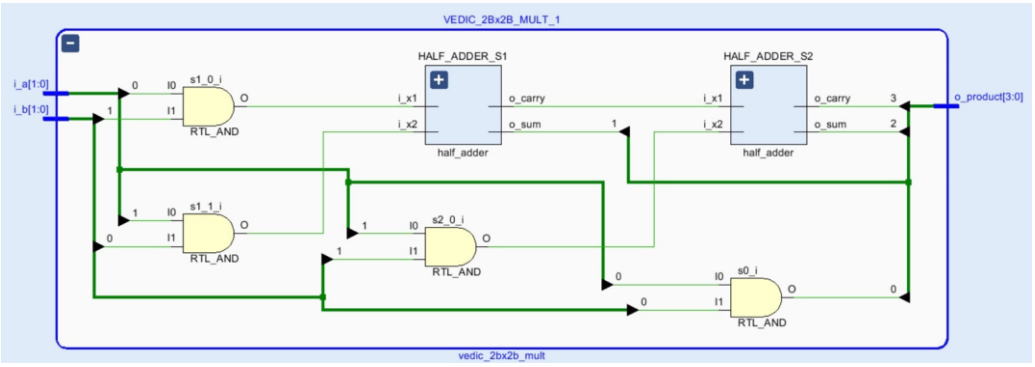

Figure.4 Schematic Results of 2-bit Multiplier using Vedic Algorithm

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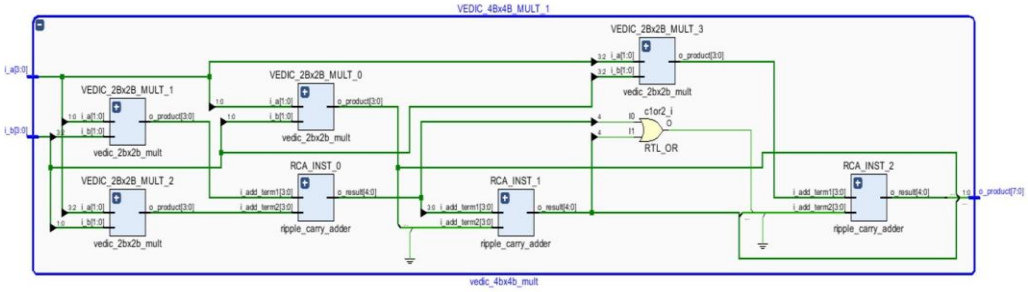

Figure.5 Schematic Results of 4-bit Multiplier using Vedic Algorithm

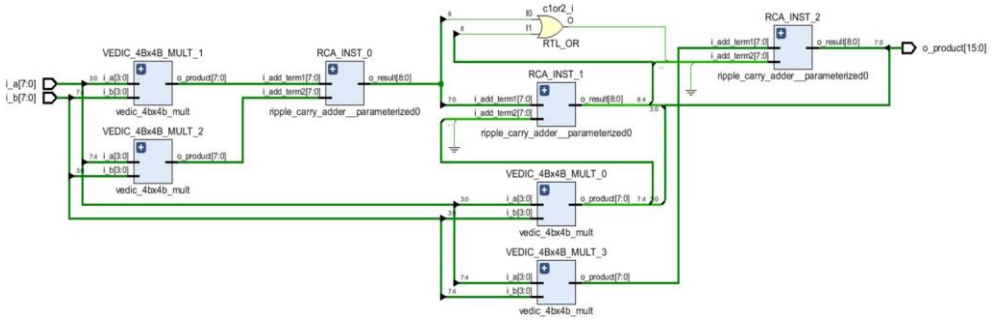

Figure.6 Schematic Results of 8-bit Multiplier using Vedic Algorithm

Area Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	104	0	303600	0.03
LUT as Logic	104	0	303600	0.03
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT6	58	LUT
LUT4	42	LUT
LUT5	20	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	10	LUT
LUT3	9	LUT

ADVANTAGES

- Improved Speed
- Reduced Area Overhead
- Low Power Consumption
- Compatibility with Modern VLSI Technologies

APPLICATIONS

Digital Signal Processing (DSP): In DSP applications like audio and video processing,real-time multiplication operations are essential for tasks such as filtering, convolution,and Fourier transforms. The efficient VLSI implementation of multipliers using the 'Urdhava Triyakbhyam'

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ISSN 2319-5991 www.ijerst.com
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algorithm can significantly enhance the speed and efficiency ofthese operations, enabling real-time processing of high-definition audio and video streams.

Communications Systems: In communication systems such as wireless networks and digital modems, multiplication operations are performed in real-time for tasks such as modulation, demodulation, and error correction coding. The efficient VLSI implementation of multipliers can improve the throughput and reliability ofcommunication systems, enabling faster data transmission rates and better signal quality.

Image and Video Processing: In applications like image and video compression, encryption, and pattern recognition, real-time multiplication operations are necessary for processing large volumes of data efficiently. The efficient VLSI implementation of multipliers can accelerate these operations, enabling real-time processing of high- resolution images and videos in applications such as surveillance, medical imaging, andvideo streaming.

Cryptography: In cryptographic applications such as encryption, decryption, and digital signatures, real-time multiplication operations are used in algorithms like RSA, ECC, and AES. The efficient VLSI implementation of multipliers can enhance the security and performance of cryptographic systems, enabling faster encryption and decryption of data in real-time.

CONCLUSION

In conclusion, the efficient VLSI implementation of 2, 4, and 8-bit multipliers using the "Urdhava Triyakbhyam" algorithm presents a promising avenue for optimizing arithmetic operations in digital circuits. Through the utilization of Vedic Mathematics principles, the proposed multipliers offer advantages in terms of reduced area, lower power consumption, and potentially higher speed compared to traditional multiplier designs.

By harnessing the inherent efficiency of the "Urdhava Triyakbhyam" algorithm,the multipliers demonstrate improved performance across various bit lengths, catering to diverse application requirements. However, challenges such as circuit complexity, timing constraints, and scalability limitations must be carefully addressed to ensure practical and reliable implementation in VLSI circuits.

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FUTURE SCOPE

Optimization for Larger Bit Widths: One potential future direction is to extend the implementation of the "Urdhava Triyakbhyam" algorithm to handle larger bit widths,such as 16-bit, 32-bit, or even higher. This would involve addressing additional challenges related to circuit complexity, timing constraints, and power consumption while maintaining efficiency.

Exploration of Faster Adder: Future research could explore using faster like CLA andother Parallel Prefix adders' techniques and methodologies to further enhance the efficiency of the "Urdhava Triyakbhyam" multiplier design.

Integration with Modern Computing Architectures: There is potential to integrate the "Urdhava Triyakbhyam" multiplier design into modern computing architectures, suchas field-programmable gate arrays (FPGAs) or application-specific integrated circuits(ASICs). This would involve adapting the design to meet the requirements of specific applications and optimizing it for seamless integration into existing systems.

Exploration of Parallel Processing Techniques: Future research could explore parallel processing techniques to further enhance the speed and efficiency of the "Urdhava Triyakbhyam" multiplier. This could involve investigating parallelization strategies at the algorithmic or circuit level to exploit parallelism and improve throughput.

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